MEMEX DOCUMENTATION

INTRODUCTION

The MEMEX is a state-of-the-art CPU Memory board capable of providing the Geneve with 2 Megabytes of 0 wait state memory. It is the subject of a new patent application and is designed around the economical 1 megabit (256k x 4 bit 80 ns) Dynamic Random Access Memory (DRAM) chips. Though these chips require complex memory refresh circuitry not needed for Static Ram (SRAM) chips, considerable economy occurs in large memory applications because DRAMS are about one fourth the cost of SRAMS on a bit for bit basis. There is also a benefit in reduced size, both resulting from the fact that DRAM chip technology requires only one transistor per bit versus 4/bit for SRAM technology.

The board was designed to be able to replace all of the 9640 address space so that even a Geneve without socketed memory can be converted to 0 wait state, nearly doubling its speed. Boards larger than 512k will require a modification to the Geneve board to bring out the two additional address lines to pins 8 and 9 of the P-Box bus, and to turn on the Geneve's bus transceiver. The information on this modification will be made available to all MEMEX purchasers as soon as the details have been worked out.

MDOS will automatically configure the added memory when booted up. There is no initialization required as with ramdisks. The basic board, with 512k installed, may be simply placed in the P—Box and can be used EXACTLY as any of the rest of the CPU memory i.e. for programs, DSK5 Ramdisk, print spooler etc. A fully loaded MEMEX may also be placed on the bus with no problems, even if the Geneve has not been modified, although the excess memory will not be accessible. The added memory can be verified by executing a "CHKDSK" from the MDOS prompt, to which MDOS will reply with "1015808 bytes of total memory" for a standard Geneve with the MEMEX as shipped (DIP Switches #1=ON, #2—#8=0FF). Better yet run MEMTEST (included), which thoroughly tests all of the 9640 memory.

In addition to MEMTEST, which will be described in more detail later, the executable package of MEMEX—DEMO is included. This is a rather elaborate graphics demo which made its debut at the 1989 Chicago Faire. It demonstrates some of what can be done on the Geneve with the added CPU memory. The demo is packaged as an archived File "MXDEMO—ARK" which contains the following Files: MEMEX—DEMO. . .MEMEX—DEMQ and VIDEO-Ol. . .VIDEO—ll. These will un-ark to 489 sectors and must all reside on the same drive for execution from the MDOS prompt matching that drive. If you have only a SSSD drive, use a "RAMDISK 152" in your AUTOEXEC and un-ark MXDEMO—ARK to DSK5.

DIP SWITCHES

The MEMEX, as shipped, assumes that you may have a card in the P—Box which does not fully decode the address bus as defined by the original TI specs. Although the 99/4A only used a 16-bit address bus, TI set aside 3 additional lines (AMA, AMB, AMC) for future expansion. Some cards, such as the CorComp disk controller and the Horizon ramdisk do not currently decode these lines (easily corrected on both cards). Normally, placing a peripheral card on the bus without taking this into account could result in damage to the bus transceiver chips on cards which would simultaneously "answer" the bus.

The MEMEX board takes care of this in two ways. First, if it detects another card answering the bus, it immediately (in a few nanoseconds) "disconnects" from the bus to prevent damage to itself or the other card. Second, a DIP switch (SW2, default=off) is provided to lock out those addresses (pages >82, >5E, >AE, >B2, >BA, >SA, >AA, >BA) which may not be decoded by such cards. The purpose of this is to avoid "confusing" current versions of MDOS which do not (as of this date) check for such cards, who's DSR's do not fully decode the bus, and could result in a memory page being mapped out by the DSR it is "talking" to. If you know that all of your cards fully decode the bus, then you may turn on SW2. This will free up 7 more pages, all but the DSR page >BA.

DIP switch #1 is for zero/one wait state mode. It ONLY affects the LED brightness. Normally this switch is ON so that 1 wait state accesses give full illumination of the LED while 0 wait state accesses give half brightness. DSR accesses will turn off the LED. This can be very useful to advanced programmers. If the Geneve is modified for 0 wait state operation, SW1 should be turned off to restore LED brightness. The MEMEX will automatically set its mode to 0 wait state when the Geneve is generating 0 wait state cycles.

Switches #3 through #8 are for the 2 Megabyte upgrade and future options. Their functions are as follows:

SW #3 ON ===> Locks out pages >E8 — >EB. . .optional Geneve 32k SRAM
SW #4 ON ===> Locks out pages >EC — >EF. . .normally Geneve 32k SRAM
SW #5 ON ===> Locks out pages >F0 — >F3 \
SW #6 ON ===> Locks out pages >F4 — >F7 POTENTIAL MDOS ROM LOCATION
SW #7 ON ===> Locks out pages >F8 — >FB or BLOCKS FOR FUTURE OPTIONS
SW #8 ON ===> Locks out pages >FC — >FF /

MEMTEST

MEMTEST is a memory diagnostic written specifically to evaluate MEMEX performance, but is applicable to any memory testing on the Geneve. Its display is organized as a graphic map of the full two megabytes of physical address space of the Geneve. This is shown as 256 banks of 8k bytes, where each column corresponds to 128k of memory. The area from page >00 thru >3F corresponds to the original 512k on board Geneve Dynamic RAM. The area from page >80 thru >BF corresponds to the location of the basic MEMEX (512k) address space. The area from page >EC thru >EF corresponds to the Geneve SRAM (fast RAM) locations and >EB thru >EB would correspond to the additional SRAM space if you have added that to your Geneve.

The area labeled "EXECUTION PAGE" shows which PHYSICAL pages are currently mapped into the 64k of TMS-9995 address space by the Geneve memory mapper. MDOS assigns these page numbers at the programmers request.

When MEMTEST loads, it asks MDOS for ALL available memory. This is where the total pages etc. info comes from. Also, when MDOS grants this request it provides a list of physical pages which have been granted. This is where the "LOCAL PAGE No." comes in, these are in essence LOGICAL page numbers. Normally local pages >00 thru >07 correspond to what PHYSICAL pages are initially loaded into the mapper (In MEMTEST local pages >O2 - >04 are not initially loaded). The remaining local pages are available for re—mapping by the programmer.