VRM 8.1 DC-DC Converter Design Guidelines

May 1997

Order Number: 243408-001

CONTENTS

This document defines DC-to-DC converters to meet the power requirements of the Intel Pentium® II processor and future microprocessors.

Each guideline is placed into one of three categories. The category immediately follows the section heading and is one of the following:

REQUIRED: An essential part of the design—necessary to meet processor voltage and current specifications.

EXPECTED: Part of Intel's standard processor power definitions; necessary for consistency with the designs of many systems and power devices.

RECOMMENDED: Normally met by of this type of DC-to-DC converter and, therefore, included as a design target. Likely to be specified by system manufacturers.

1.0. ELECTRICAL SPECIFICATIONS

The DC-DC converter supplies the required voltage and current to a processor as shown in Table 1 or Table 2.

Table 1. Pentium® II Processor Voltage and Current Specifications[1]

Symbol	Parameter	Processor core frequency (MHz)[2]	Minimum	Typical	Maximum	Unit
Vcc_{CORE}	Vcc for processor core			2.8		V
	Vcc_{CORE} static tolerance		–0.060		0.100	V
	Vcc_{CORE} transient tolerance	233 266 300	–0.140 –0.140 –0.130		0.140 0.140 0.130	V V V
Icc_{CORE}[3]	Current for Vcc_{CORE}	233 266 300		6.9 7.8 8.7	11.8 12.7 14.2	A A A
$Icc_{SGNTCORE}$	Icc for Stop-Grant Vcc_{CORE}	233 266 300		0.80 0.90 TBD	1.1 1.2 TBD	A A A
$Icc_{SLPCORE}$	Icc for Sleep Vcc_{CORE}			.070	.080	A
$Icc_{DSLPCORE}$	Icc for Deep Sleep Vcc_{CORE}				.020	A
$dIcc_{CORE}/dt$	Icc slew rate				30	A/µs

Table 2. Voltage and Current Specifications for Future Processors[1,4]

Symbol	Parameter	Processor core frequency (MHz)[2]	Minimum	Typical	Maximum	Unit
Vcc_{CORE}	Vcc for processor core			1.8 2.0		V
	Vcc_{CORE} static tolerance		–0.060		0.100	V
	Vcc_{CORE} transient tolerance		-0.100		0.100	V
Icc_{CORE}[3]	Current for 1.8 V Vcc_{CORE} Current for 2.0 V Vcc_{CORE}	TBD			10.2 11.3	A A
$Icc_{SGNTCORE}$	Icc for Stop-Grant Vcc_{CORE}	TBD		TBD	TBD	A
$Icc_{SLPCORE}$	Icc for Sleep Vcc_{CORE}			TBD	TBD	A
$Icc_{DSLPCORE}$	Icc for Deep Sleep Vcc_{CORE}				TBD	A
$dIcc_{CORE}/dt$	Icc slew rate				20	A/µs

NOTES:

1. All parameters measured at VRM pins on system board.
2. Specifications apply to all frequencies unless specific frequencies are listed.
3. $I_{cc}CORE$ measured at nominal $V_{CC}CORE$ under maximum signal loading conditions.
4. Includes Pentium® II processor flexible motherboard applications.

1.1. Input Voltage and Current

- **Input Voltages** **EXPECTED**

Available inputs are at 12V ±5% and 5V ±5%. Any single voltage or combination may be used by the converter. These voltages are supplied by a conventional desk-top computer power supply through a cable to the motherboard. Input voltage requirements should be clearly marked on the module.

- **Load Transient Effects on Input Voltages** **RECOMMENDED**

The converter should be able to provide for an output current step at the load from Icc_{CORE} (Stop-Grant state) to Icc_{CORE} (Maximum) or Icc_{CORE} (Maximum) to Icc_{CORE} (Stop-Grant state) within the time interval listed in Section 1.3. During this step response the input current di/dt should not exceed 0.1A/µsec. For applications with multiple converters, it is recommended that the step response di/dt of an individual converter not exceed 0.04A/ µsec.

1.2. Input Controls

These are signals that control the DC-to-DC converter (shown with corresponding pins in Table 4).

- **Output Enable—OUTEN** **EXPECTED**

The module should accept an open collector signal consistent with TTL DC specifications for controlling the output voltage: The logic low state disables the output voltage.

- **Voltage Identification—VID[0:4]** **EXPECTED**

The module should accept five signals, used to indicate the voltage required by the processor, as defined by Table 3. Five processor package pins will have an open–ground pattern corresponding to the voltage required by the individual processor unit. System designs may use pull-ups to the input voltage, with an appropriate resistor divider if using a 12V input. If used, such pull-ups should have a resistance ≥ 10KΩ. Voltages above 2.8V may be considered optional for use by the module supplier and system manufacturer. The module output should be disabled for voltages below 1.8V.

1.3. Output Requirements

- **Static Voltage Regulation** **REQUIRED**

The output voltage measured at the converter output pins on the system board must be within the static range shown in Table 1-1, except for input voltage turn-on and turn-off and for current transitions as shown under "Transient Voltage Regulation" below. The static limits apply to ambient temperatures between 0°C and 60°C. Static voltage regulation includes:

  — DC output initial voltage set point adjust
  — Output ripple and noise
  — Output load ranges specified in Table 1
  — Temperature and warm up specified in Section 3.1.

- **Transient Voltage Regulation** **REQUIRED**

The output voltage measured at the converter output pins on the system board must be within the transient range shown in Table 1, including the transition from Icc_{SGNT}CORE (Stop-Grant state) to Icc_{CORE} (Maximum) or from Icc_{CORE} (Maximum) to Icc_{SGNT}CORE (Stop-Grant state), except as noted for input voltage turn-on and turn-off. This tolerance must include the variation due to DC voltage regulation plus the effects of an output load transient (slew rate) of 30A/µsec at the converter output pins. Load transient response may not exceed the static voltage specification for longer than 2 microseconds. The toggle rate for the output load transition must range from 100 Hz to 100 kHz. Under the above conditions and for all toggle rates, the transient response must be measured over a 20 MHz frequency band, and at ambient temperatures between 25°C and 50°C.

Table 3. Voltage Identification Code

Processor Pins 0 = Connected to Vss 1 = Open or pull-up to Vin						Processor Pins 0 = Connected to Vss 1 = Open or pull-up to Vin					
VID4	VID3	VID2	VID1	VID0	(VDC)	VID4	VID3	VID2	VID1	VID0	(VDC)
0	1	1	1	1	*	**1**	**1**	**1**	**1**	**1**	**No CPU**
0	1	1	1	0	*	**1**	**1**	**1**	**1**	**0**	**2.1**
0	1	1	0	1	*	**1**	**1**	**1**	**0**	**1**	**2.2**
0	1	1	0	0	*	**1**	**1**	**1**	**0**	**0**	**2.3**
0	1	0	1	1	*	**1**	**1**	**0**	**1**	**1**	**2.4**
0	1	0	1	0	*	**1**	**1**	**0**	**1**	**0**	**2.5**
0	1	0	0	1	*	**1**	**1**	**0**	**0**	**1**	**2.6**
0	1	0	0	0	*	**1**	**1**	**0**	**0**	**0**	**2.7**
0	0	1	1	1	*	**1**	**0**	**1**	**1**	**1**	**2.8**
0	0	1	1	0	*	1	0	1	1	0	2.9
0	**0**	**1**	**0**	**1**	**1.80**	1	0	1	0	1	3.0
0	**0**	**1**	**0**	**0**	**1.85**	1	0	1	0	0	3.1
0	**0**	**0**	**1**	**1**	**1.90**	1	0	0	1	1	3.2
0	**0**	**0**	**1**	**0**	**1.95**	1	0	0	1	0	3.3
0	**0**	**0**	**0**	**1**	**2.00**	1	0	0	0	1	3.4
0	**0**	**0**	**0**	**0**	**2.05**	1	0	0	0	0	3.5

NOTES:

* Level reserved for future requirements; VRM8.1 output should be disabled for these VID codes.

- **Output Ripple and Noise** **RECOMMENDED**

Ripple and noise are defined as periodic or random signals over a 20 MHz frequency band at the output pins under constant load. Output ripple should be consistent with the static voltage requirements.

- **Variation with Load** **RECOMMENDED**

To assist in providing margin during high slew rate current load transitions, the vendor may target module performance so as to provide for a nominal +40 mV offset when under minimum load conditions, and a nominal –40 mV offset when under maximum load conditions.

- **Turn-on Response Time** **RECOMMENDED**

The output voltage should be within its specified range within 10 msec of the input reaching 95% of its nominal voltage.

- **Overshoot at Turn-On or Turn-Off** **REQUIRED**

Overshoot upon the application or removal of the input voltage under the conditions specified in Section 1.1 must be less than 10% above the initial set output voltage. No negative voltage may be present on any output during turn-on or turn-off.

- **Power Good Output—PWRGD** **EXPECTED**

An open collector signal consistent with TTL DC specifications should be provided. This signal should transition to the open (>100KΩ) state within 20 milliseconds of the input stabilizing within the range specified in Section 1.1. The signal should be in the low-impedance (to ground) state whenever Vout is more than ±12% from nominal and be in the open state whenever Vcc_{CORE} is within its specified range.

1.4. Efficiency

RECOMMENDED

The efficiency of the DC-to-DC converter should be greater than:

- 80% at maximum output current
- 40% at 0.5A.

1.5. Protection

These are features built into the DC-to-DC converter to prevent damage to itself or the circuits it powers.

- **Over Voltage Protection** **RECOMMENDED**

Protection Level: The converter should provide over-voltage protection by shutting itself off when the output voltage rises beyond Vtrip. Vtrip should be set between 110% and 125% of the voltage demanded by the processor (via the VID pins).

Voltage Sequencing: No combination of input voltages should falsely trigger an OVP event.

- **Short Circuit Protection** **RECOMMENDED**

Load short circuit is defined as a load impedance of less than approximately 100 mΩ. The DC-to-DC converter should be capable of withstanding a continuous short-circuit to the output without damage or over-stress to the unit.

- **Reset After Shutdown** **RECOMMENDED**

If the DC-to-DC converter goes into a shutdown state due to a fault condition on its outputs, the DC-to-DC converter should return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.

1.6. Current Sharing

RECOMMENDED

The pin designated Ishare is intended to permit two or more modules (from the same vendor) to balance the total current load between them. The sharing mechanism is left open for specific module or system implementations.

2.0. MECHANICAL REQUIREMENTS

The VRM 8.1 converter interface should be mechanically compatible with Intel's Voltage Regulator Module Header 8, revision 3.0 (per Figure 5).

- **Dimensions** **EXPECTED**

Outline dimensions should be equal to or less than 3.1" x 1.5" x 1.1". Maximum component height should be 0.90" on the connector side and 0.14" on the back side of the module (ref. Figure 2).

- **Interconnect** **EXPECTED**

Interconnect should consist of a 40 pin interface, type AMPMOD2 or equivalent, with the socket (part number 532956-7 or equivalent) mounted to the module (per Figure 3). The current capacity must be at least 2A/pin. The pin electrical interface should be as given in Table 4.

Table 4. Module Pinout

Pin #	Row A	Row B
1	5Vin	5Vin
2	5Vin	5Vin
3	5Vin	Reserved[1]
4	12Vin	12Vin
5	Reserved[2]	Reserved
6	Ishare	OUTEN
7	VID0	VID1
8	VID2	VID3
9	VID4	PWRGD
10	Vcc_{CORE}	Vss
11	Vss	Vcc_{CORE}
12	Vcc_{CORE}	Vss
13	Vss	Vcc_{CORE}
14	Vcc_{CORE}	Vss
15	Vss	Vcc_{CORE}
16	Vcc_{CORE}	Vss
17	Vss	Vcc_{CORE}
18	Vcc_{CORE}	Vss
19	Vss	Vcc_{CORE}
20	Vcc_{CORE}	Vss

1. Some systems may connect pin B3 to 5Vin for compatibility with future VRM pinouts.
2. Some systems may connect pin A5 to 12Vin for compatibility with future VRM pinouts.

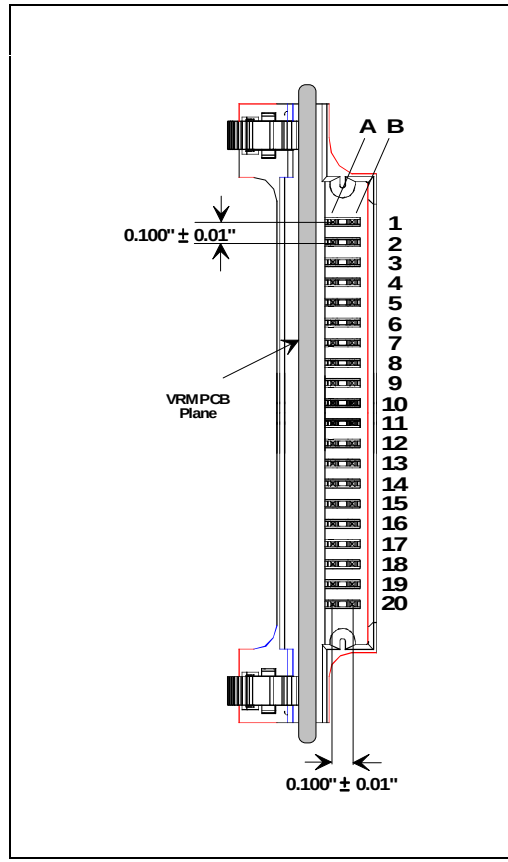

Figure 1. Pin Orientation

- **Mating header (reference)**

The VRM 8.1 Header is a 40-position, two-row shrouded header with straight posts on 0.1 inch centers (ref. AMP # 146315-1 or equivalent). The voltage regulator module is to be retained to and removed from the header by features on the header that mate with the voltage regulator module. The removal and installation process must not require the use of tools. The removal features must be accessible from the back side (opposite the receptacle) of the module. (ref. Figure 1 and Figure 5).

- **Weight** **EXPECTED**

Package weight, including any integral heat sink, should be less than three ounces.

- **Marking** **EXPECTED**

The input voltage (either +5VDC or +12VDC) should be conspicuously marked on the module, to be visible during insertion of the module into the header. Marking options include:

  — Color code the text on the label: red = +5V; blue = +12V.

  — List the output voltage range and input and output currents.

- Alternative attachment (reference)

Normally the module should be capable of being inserted and extracted from the top, without the use of any tools. An alternative mounting configuration, as shown in Intel application note AP-523, *Pentium® Pro Processor Power Distribution Guidelines*, is permitted. In this configuration the baseboard interface should consist of an unshrouded connector type AMPMOD2, part number 2-103783-0, or equivalent. This mounting configuration is recommended for applications where, under normal usage, the module would not be removed after installation.

3.0. TESTS AND STANDARDS RECOMMENDED

3.1. Environmental

Design, including materials, should be consistent with the manufacture of units that meet the environmental standards in Table 5.

Table 5. Environmental Specifications

	Operating	**Non-Operating**
Temperature	Ambient 0°C to +60°C at full load with a maximum rate of change of 5°C/10 minutes minimum but no more than 10°C/hour. [1]	Ambient –40°C to 70°C with a maximum rate of change of 20°C/hour. [2]
Humidity	To 85% relative humidity.	To 95% relative humidity.
Altitude	0 to 10,000 feet	0 to 50,000 feet.
Electrostatic discharge	15 KV initialization level. The direct ESD event shall cause no out-of-regulation conditions. [3]	25 KV initialization level.

1. See Section 1.3 for static and transient test condidtions.
2. Thermal shock of –40°C to +70°C, 10 cycles; transfer time shall not exceed 5 minutes, duration of exposure to temperature extremes shall be 20 minutes.
3. Includes overshoot, undershoot, and nuisance trips of the over-voltage protection, over-current protection or remote shutdown circuitry.

3.2. Shock and Vibration

The DC-to-DC converter should not be damaged and the interconnect integrity not compromised during:

- A shock of 50G with an 11 millisecond half sine wave, non-operating, the shock to be applied in each of the orthogonal axes.
- Vibration of $0.01G^2$ per Hz at 5 Hz, sloping to $0.02G^2$ per Hz at 20 Hz and maintaining $0.02G^2$ per Hz from 20 Hz to 500 Hz, non-operating, applied in each of the orthogonal axes.

3.3. Electromagnetic

Design, including materials, should be consistent with the manufacture of units that comply with the limits of FCC Class B and VDE 243 Level B for radiated emissions, given the existence of an external package around the converter with 20dB of shielding.

3.4. Reliability

The converter should be designed to function to electrical specifications, within the environmental specifications, with 60°C air at a velocity of 100 LFM directed along the connector axis.

- Component De-rating

The following component de-rating guidelines should be followed:

  - Semiconductor junction temperatures should be < 115°C with ambient at 50°C.
  - Capacitor case temperature should not exceed 80 % of rated temperature.
  - Resistor wattage de-rating should be > 50%.
  - Component voltage and current de-rating should be > 20%, the effects of ripple current heating should be accounted for in this de-rating.
- Mean-Time-Between-Failures (MTBF)

Design, including materials, should be consistent with the manufacture of units with an MTBF of 500,000 hours of continuous operation at 55°C, maximum-outputs load, and worst-case line, while meeting specified requirements. MTBF should be calculated in accordance with MIL-STD-217F.

3.5. Safety

Design, including materials, should be consistent with the manufacture of units that meet the standards of UL flammability specifications per 94V-0.

4.0. PHYSICAL DIMENSIONS

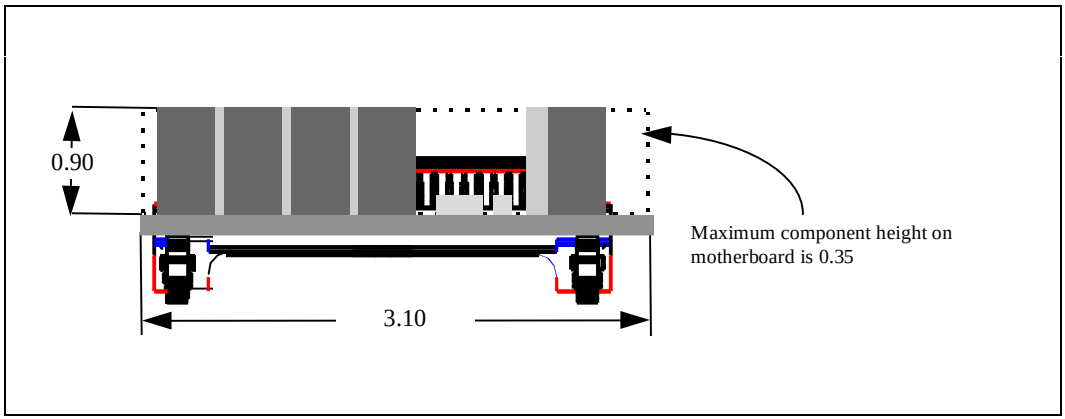

Figure 2. Module Top View (dimensions in inches)

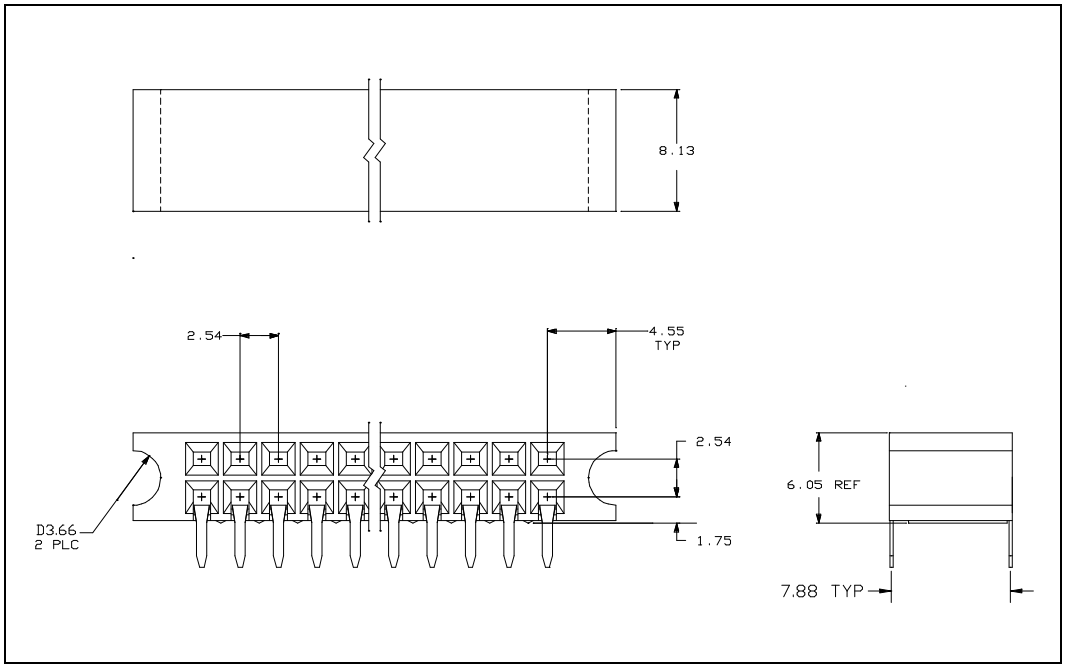

Figure 3. Module Connector Features (dimensions in mm)

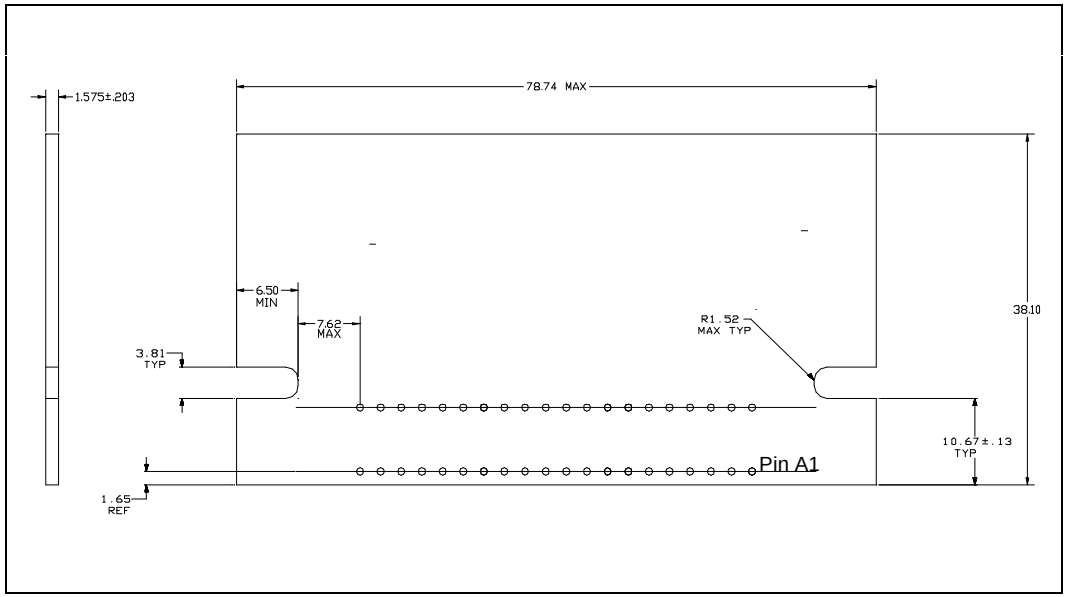

Figure 4. Voltage Regulator Module Printed Wiring Board Features (Viewed from connector side, dimensions in mm)

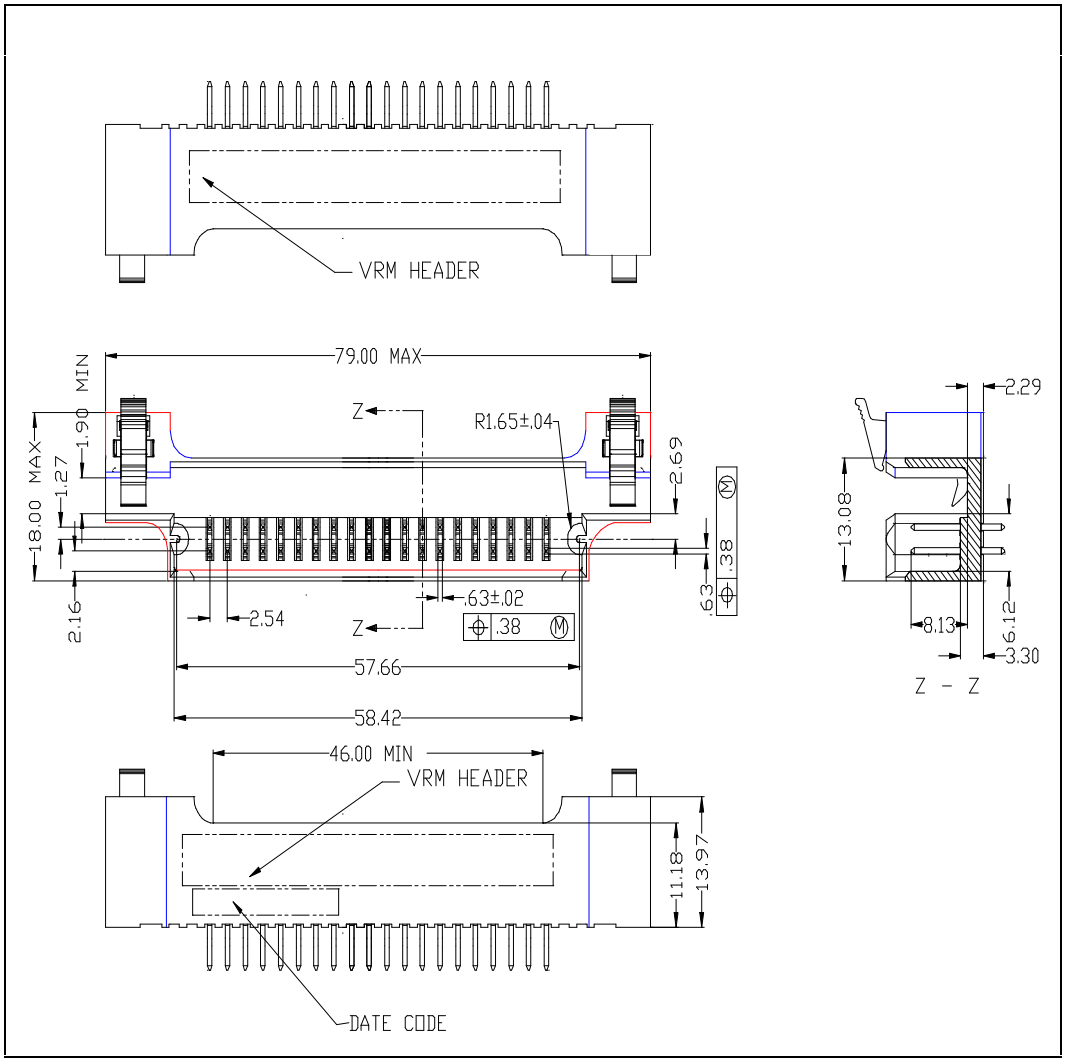

Figure 5. Mating Header
(dimensions in mm)