Developer Note

Power Macintosh G3

Developer Note

Technical Publications

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Contents

Preface About This Note 11

Topics Described In This Note 11
Supplemental Reference Documents 12
PowerPC Microprocessor 12
Mac OS 12
Open Firmware 13
PCI Cards 14
ATA Devices 14
USB Devices 14
FireWire Interface 15

Chapter 1 Introduction 17

Power Macintosh G3 Computer Features 18
Features of the Enclosure 20
Front View of the Enclosure 21
Back View of the Enclosure 22
Access to the Interior 23
Optional Features 25
DVD-ROM and DVD MPEG2 Decode Card 25
Serial Modem Communications 26
Compatibility Issues 26
System Software 26
DMA Addresses and NewWorld Software 26
Machine Identification and NewWorld Software 26
No Graphics Support on MLB 27
No Built-in AV I/O Connectors 27
Modem Slot 27
PCI Expansion Slots 27
Internal Storage Devices 28
RAM Expansion 28
No L2 Cache Expansion 29

ATA-3 Drives 29
No SCSI Ports 29
Line Voltages 29
Monitor Power 29
No Video RAM Expansion 30
No LocalTalk Serial Ports 30
USB Ports and Devices 30

Chapter 2 Architecture 31

Block Diagram and Buses 32
Main Components 34
PowerPC G3 Microprocessor 34
Memory Subsystem 34
Second-Level Cache 35
System ROM 35
System RAM 35
Core ICs 35
Grackle Memory Controller and PCI Bridge IC 36
Paddington I/O Controller IC 37
Burgundy Sound IC 37
Cuda IC 38
Graphics Controller IC 38
Display Memory 39
USB Controller 39
FireWire Link Controller 40
Optional Internal Modem 40

Chapter 3 I/O Features 41

ADB Port 42
USB Ports 43
USB Connectors 44
Transfer Types Supported 44
USB Compatibility Issues 45
ADB Compatibility 45

Serial Port Compatibility 45
Macintosh-To-Macintosh Connections 46
USB Storage Devices 46
USB Controller 46
Keyboard 46
Keyboard Layout 46
Keyboard and USB 47
Mouse 48
FireWire Ports 48
FireWire Connector 49
Ethernet Port 50
Internal Modem 50
Disk Drives 51
Ultra DMA / 33 Hard Disk Drive 52
Optional Ultra2 SCSI (LVD) Drive 52
ATAPI CD-ROM Drive 52
Optional ATAPI Zip Drive 53
Optional DVD-ROM Drive 53
Sound System 53
Sound Outputs 53
Sound Inputs 54
Digitizing Sound 54
Video Monitor Port 55
Graphics Card 55
Monitor Connector 56
Monitor Adapter 57
Monitor Sense Codes 57
Display Resolution Modes 59
Graphics Acceleration Display Modes 61

Chapter 4 Expansion Features 63

RAM DIMMs 64
Mechanical Specifications 64
Presence Detect EEPROM 65
RAM Address Multiplexing 65
SDRAM Devices 66

PCI Expansion Slots 66
The Modem Interface 67

Chapter 5 System Software 69

The New Approach 70
What Has Changed 71
Features of the New Approach 72
Performance 72
RAM Footprint 73
User Experience 73
Data Structures and Files 73
Compatibility 73
Boot ROM Contents 74
POST Code 75
Open Firmware 75
Mac OS 'ndrv' Drivers 75
RTAS 76
Mac OS ROM Image File Contents 76
Open Firmware Script 77
Trampoline Code 77
Mac OS ROM Image 77
NewWorld Boot Process 77
What Is Different 78
Interrupt Handling 79
Outmoded Resources 79
RAM Footprint 79
RTAS 79
NV-RAM 80
NanoKernel 80
Startup Disk Control Panel 80
Open Firmware and the Device Tree 81
Open Firmware and Startup Devices 81
Interrupt Layout 82
Machine Identification 82

Appendix A Conventions and Abbreviations 85

Typographical Conventions 85
Abbreviations 85

Index 89

Figures and Tables

Chapter 1 Introduction 17

Figure 1-1 Front view of the enclosure 21
Figure 1-2 Back view of the enclosure 22
Figure 1-3 Opening the side panel 23
Figure 1-4 Interior of the computer 24
Figure 1-5 Closing the side panel 25

Chapter 2 Architecture 31

Figure 2-1 Main logic board block diagram 33

Chapter 3 I/O Features 41

Figure 3-1 ADB connector 42
Figure 3-2 ANSI keyboard layout 47
Figure 3-3 FireWire connector 49
Figure 3-4 Monitor connector 56

Table 3-1 ADB connector pin assignments 43
Table 3-2 USB connector pin assignments 44
Table 3-3 FireWire connector pin assignments 49
Table 3-4 Monitor connector pin assignments 56
Table 3-5 Monitor sense codes 58
Table 3-6 Supported display resolutions 59
Table 3-7 Supported graphics acceleration display modes 61

Chapter 4 Expansion Features 63

Table 4-1 Address multiplexing modes for SDRAM DIMMs 65

About This Note

This developer note describes a new Macintosh computer. The computer is referred to as the Power Macintosh G3 throughout the developer note. Where necessary, the term “original Power Macintosh G3” is used to refer to the earlier models.

This note describes the features of the Power Macintosh G3 computer, the logic board architecture and expansion capabilities, and issues affecting compatibility.

This developer note is intended to help hardware and software developers design products that are compatible with the Macintosh products described here. If you are not already familiar with Macintosh computers or if you would simply like additional technical information, you may wish to read the related technical manuals listed in the section “Supplemental Reference Documents.”

This note is published only in electronic form, as an Adobe™ Acrobat™ PDF (portable document format) file and in HTML for browsers that support frame sets. The file is available from two sources:

- on the World Wide Web at <http://developer.apple.com/techpubs/hardware/hardware.html>
- on the Reference Library Edition of the Developer CD Series, which is distributed as part of the monthly mailing to registered developers

Topics Described In This Note

The information is arranged in five chapters, an appendix, and an index:

- Chapter 1, “Introduction,” gives a summary of the features of the logic board in the Power Macintosh G3 computer, describes the physical appearance of the enclosure, and lists the available configurations and options. This chapter also includes a section describing compatibility issues that developers need to be aware of to take advantage of the features available with the Power Macintosh G3 computer.

- Chapter 2, “Architecture,” describes the internal organization of the computer. It includes a functional block diagram and descriptions of the main components of the logic board.
- Chapter 3, “I/O Features,” describes the built-in input/output (I/O) devices and the external I/O ports. It also describes the built-in support for external video monitors that can be used with the computer.
- Chapter 4, “Expansion Features,” describes the expansion slots on the logic board and provides descriptions of the expansion modules.
- Chapter 5, “System Software,” describes the system software that comes with the computer, with emphasis on the new Open Firmware features.
- Appendix A, “Conventions and Abbreviations,” describes the typographical conventions and lists the abbreviations used in this note.

Supplemental Reference Documents

For more information about the technologies mentioned in this developer note, you may wish to consult some of the references listed in the following sections.

PowerPC Microprocessor

For more information about the PowerPC™ 750 microprocessor used in the Power Macintosh G3 computer, you may wish to refer to the standard reference, PowerPC 740/750 Microprocessor Implementation Definition Book IV. Information about the PowerPC 750 microprocessor is also available on the World Wide Web at

http://www.mot.com/SPS/PowerPC/index.html

and

http://www.chips.ibm.com/products/ppc/overview

Mac OS

For a description of the version of the Mac OS that comes with the new models, refer to the Apple Technical Note for Mac OS 8.5. The Technote is available on the Technote Web site at

http://developer.apple.com/technotes/index.html

You should also have copies of the relevant books describing the system software for Macintosh computers available in technical bookstores and on the World Wide Web at

http://developer.apple.com/techpubs/mac/mac.html

Open Firmware

The NewWorld software architecture implemented on the Power Macintosh G3 computer follows some of the standards defined by the Open Firmware IEEE 1274-1995 specification and the CHRP binding.

The primary Open Firmware reference is the IEEE 1275-1994 Standard for Boot (Initialization, Configuration) Firmware: Core Requirements and Practices. You can order that document electronically from the IEEE Standards Department web site at

http://standards.ieee.org/catalog/bus.html

or you can order it by mail from

IEEE Standards Department
445 Hoes Lane, P. O. Box 1331
Piscataway, NJ 08855-1331
Telephone 800-678-4333 (US), 908-562-5432 (International)

The basis for the bootinfo file format and its use are described the document PowerPC Microprocessor Common Hardware Reference Platform (CHRP) System binding to: IEEE Std 1275-1994 Standard for Boot (Initialization, Configuration) Firmware. A bootinfo file contains Open Firmware script, a description, information for individual operating systems, and icons, along with other information.

An introduction to Open Firmware as used with PCI expansion cards on the Macintosh computer is given in *Designing PCI Cards and Drivers for Power Macintosh Computers.*

Three Apple Technical Notes provide additional information about Open Firmware on the Macintosh computer. They are

- TN 1061: Open Firmware, Part I, which introduces Forth programming and outlines a technique for debugging Open Firmware drivers. It is available on

the Technote Web site at
http://developer.apple.com/technotes/tn/tn1061.html

- TN 1062: Open Firmware, Part II, which describes the contents of an expansion ROM for Open Firmware and lists properties common to all device types. It is available on the Technote Web site at
http://developer.apple.com/technotes/tn/tn1062.html
- TN 1044: Open Firmware, Part III, which describes a typical device tree. It is available on the Technote Web site at
http://developer.apple.com/technotes/tn/tn1044.html

PCI Cards

For information about PCI expansion cards, refer to *Designing PCI Cards and Drivers for Power Macintosh Computers*. The Power Macintosh G3 computer supports version 2.1 of the PCI standard.

If you're interested in taking advantage of the 3D graphics acceleration features available on the PCI graphics card, you should have a copy of *3D Graphics Programming With QuickDraw 3D*.

ATA Devices

For the latest information about the Mac OS software for ATA devices, see ATA Software Guide and ATA Device 0/1 Software Developers Guide, available on the World Wide Web at:

http://developer.apple.com/techpubs/hardware/hardware.html

USB Devices

For more information about the Universal Serial Bus (USB) on the Macintosh computer, refer to Apple Computer's USB DDK API Reference. Information is also available on the World Wide Web, at

http://developer.apple.com/dev/usb/

For full specifications of the Universal Serial Bus, developers should refer to the USB Implementation Forum on the World Wide Web, at

http://www.usb.org/developers/index.html

FireWire Interface

For additional information about the FireWire IEEE 1394 interface and the Apple APIs for FireWire software, refer to the resources available on the Apple FireWire Web site at

http://www.apple.com/firewire/

The IEEE 1394-1995 standard is available from the IEEE. Ordering information can be found on the World Wide Web at

http://www.ieee.org

You may also find useful information at the 1394 trade association's Web site at

http://www.1394ta.org/

CHAPTER 1

Introduction

The Power Macintosh G3 computer is a new computer with a higher speed CPU and system bus and several new built-in I/O features that allow customers to assemble powerful and versatile Macintosh configurations.

Power Macintosh G3 Computer Features

Here is a list of the hardware features of the Power Macintosh G3 computer. The major features are described more fully later in this note.

- **Microprocessor:** PowerPC G3 microprocessor running at a clock frequency of 300 MHz, 350 MHz, or 400 MHz depending on model and configuration. For more information, see "PowerPC G3 Microprocessor" (page 34).
- **Cache:** 512 KB or 1 MB (depending on model and configuration) of the backside second-level (L2) cache on processor module. The backside cache runs at half the clock frequency of the microprocessor.
- **Processor system bus:** 64-bit wide data and 32-bit wide address, 100 MHz clock, supporting split address and data tenures.
- **RAM:** four DIMM slots for industry standard PC-100 SDRAM (synchronous dynamic access memory) DIMMs (dual inline memory modules). Maximum memory with all four slots occupied is 1024 MB. A minimum of 64 MB of RAM is installed in one of the slots. For more information, see "RAM DIMMs" (page 64).
- **ROM:** New World ROM-in-RAM implementation with 1 MB of boot ROM. For additional information about the ROM, see "System ROM" (page 35) and "Boot ROM Contents" (page 74).
- **Graphics acceleration:** 2D and 3D hardware graphics acceleration using the ATI 3D RAGE 128 GL graphics controller on the 66 MHz 2D/3D accelerated graphics card. Software support through Macintosh QuickDraw 3D and QuickDraw 3D RAVE (rendering acceleration virtual engine) APIs. For more information, see "Graphics Card" (page 55).
- **Sound:** supports 16 bits/channel stereo input and output on built-in 3.5mm line-level stereo input and output jacks, one built-in speaker. For more information, see "Sound System" (page 53).
- **Hard disk drives:** one internal Ultra DMA/33 hard disk or Ultra2 SCSI (LVD) hard disk. For more information, see "Disk Drives" (page 51).

- **Drive bays:** three drive bays, one of which is occupied by an Ultra DMA / 33 hard disk or an Ultra2 SCSI (LVD) hard disk. The other two bays are available for adding other devices connected to a PCI controller card. For more information, see “Disk Drives” beginning on page 51.
- **CD-ROM drive:** internal 24x-speed ATAPI CD-ROM drive.
- **DVD-ROM drive:** optional ATAPI DVD-ROM drive providing support for 32x-speed CD-ROM and 5x-speed DVD-ROM media, as well as DVD-Video playback with the DVD MPEG2 decode module. The DVD MPEG2 decode module is connected to the PCI graphics card.
- **Zip drive:** optional 100 MB ATAPI Zip drive. If the Zip drive option is not installed at the time of purchase, data and power connectors are provided to add an ATAPI Zip drive to the system.
- **USB ports:** two USB ports, described in “USB Ports” (page 28). The computer comes with a USB mouse and a USB keyboard that has two additional USB ports. The additional ports are described under “Keyboard and USB” (page 47).
- **ADB port:** one ADB port for ADB devices or ColorSync control of Apple monitors. For more information, see “ADB Port” (page 42).
- **Ethernet:** built in Ethernet port for 10Base-T and 100Base-TX operation with an RJ-45 connector. For more information, see “Ethernet Port” (page 50).
- **FireWire ports:** two IEEE-1394 high-speed serial FireWire ports, which support transfer rates of 100, 200, and 400 Mbps.
- **Modem:** optional Apple 56 Kbps modem. The modem supports K56flex and V.90 protocols. For more information, see “Internal Modem” (page 50).
- **Keyboard:** Apple USB keyboard with function keys and inverted-T cursor motion keys. The keyboard operates as a low-speed (1.5 Mbps) USB device. It also provides a bus-powered USB hub with two USB ports. For more information, see “Keyboard” (page 46).
- **Mouse:** Apple USB mouse operating as a low-speed (1.5 Mbps) USB device. For more information, see “Mouse” (page 48).
- **PCI card expansion slots:** three slots for 33 MHz, 32-bit or 64-bit, 12-inch PCI cards; one slot for a 66 MHz 32-bit PCI card, occupied by the accelerated graphics card. For more information, see “PCI Expansion Slots” (page 66).
- **Power switch:** soft power controlled from the Apple USB keyboard, an ADB keyboard, and the front power button.

- **Voltage switch:** can be set to either 115 for voltages of 90-132 V or 230 for voltages of 180-264 V, depending on the voltage where the computer is installed. The voltage selection must be set manually.
- **Fan speed control:** The speed of the fan is thermally controlled and is automatically set to the lowest possible speed to minimize noise. The fan speed varies according to the temperature inside the enclosure. This is a function provided by the fan and is not under software control.
- **Energy saving:** sleep, startup, and shutdown scheduling can be controlled with an Energy Saver control panel.

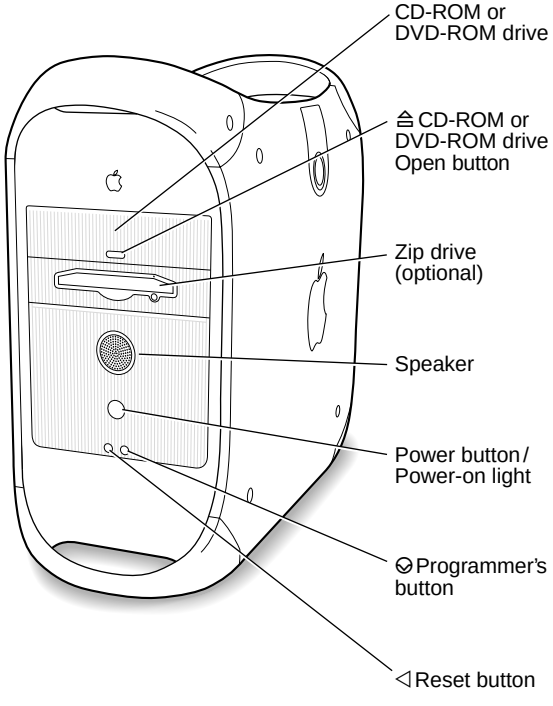
Features of the Enclosure

The Power Macintosh G3 enclosure is a new design. The following sections show the exterior design and the interior of the computer.

Front View of the Enclosure

Figure 1-1 is a front view of the Power Macintosh G3 enclosure. The front view shows the openings for the CD/DVD-ROM drive and the optional ZIP drive, the speaker, the power button, the reset button, the NMI button, and the power-on light.

Figure 1-1 Front view of the enclosure

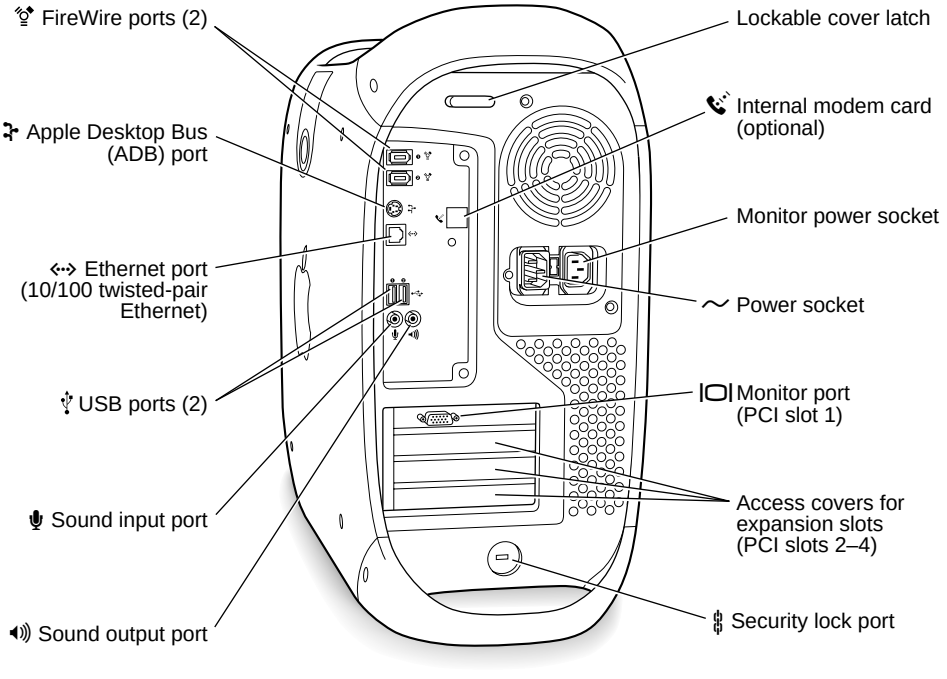


Back View of the Enclosure

The back panel includes the A/C power socket, the monitor power socket, the I/O ports, and the openings for PCI cards.

Figure 1-2 shows the back view of the enclosure for the Power Macintosh G3 computer.

Figure 1-2 Back view of the enclosure



Access to the Interior

You can get access to the interior of the computer to add expansion RAM or PCI expansion cards by opening the side panel as shown in Figure 1-3. A view of the interior is shown in Figure 1-4. Figure 1-5 shows the proper way to close the side panel.

Figure 1-3 Opening the side panel

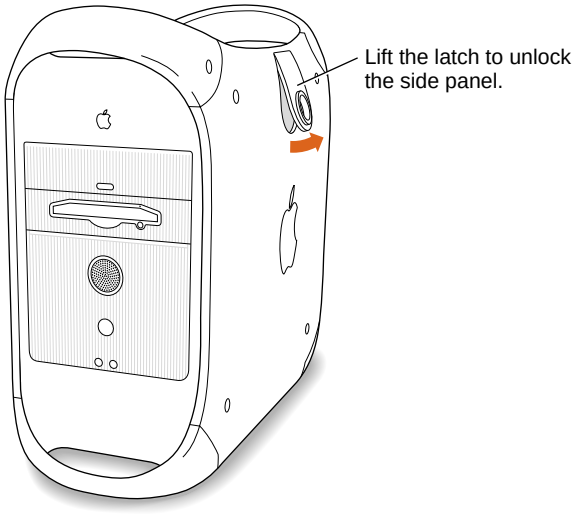


Figure 1-4 Interior of the computer

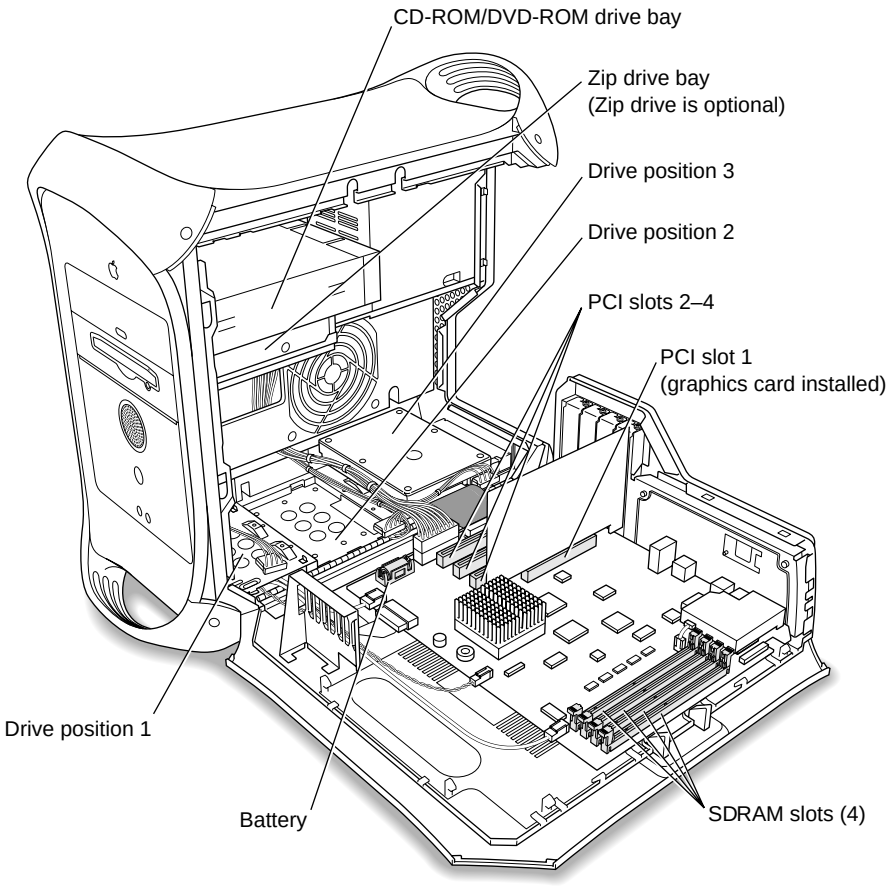
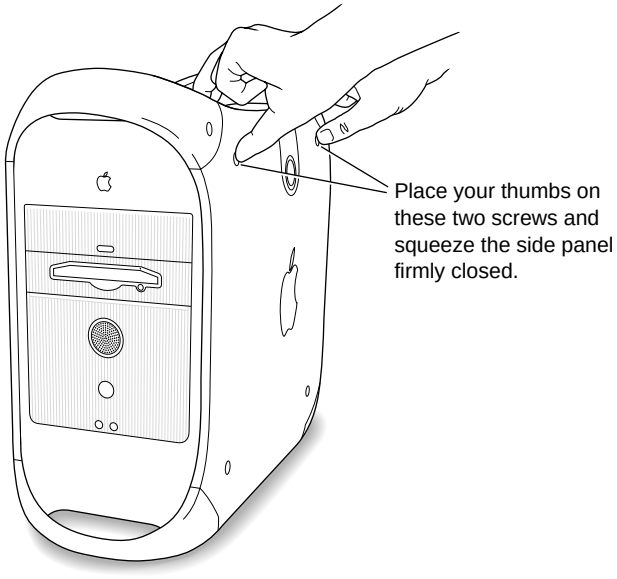


Figure 1-5 Closing the side panel



Optional Features

Two features of the computer are implemented as plug-in modules available as a configuration option at the time of purchase.

DVD-ROM and DVD MPEG2 Decode Card

The DVD-ROM drive configuration includes a DVD MPEG2 decode card module. That module does not occupy a PCI slot, but is attached to the accelerated graphics card.

The DVD MPEG2 decode card module supports viewing DVD video movies on a monitor connected to the 15-pin video output port on the PCI 2D/3D accelerated graphics card. DVD digital audio from the DVD media is sent to a DAC (digital-to-analog converter) and then to the Burgundy IC for analog stereo sound output to the currently selected sound output port.

Serial Modem Communications

An internal Apple 56 Kbps modem can be installed as an option at the time of purchase. The modem is compatible with K56flex, V.34, and V.90 protocols.

Compatibility Issues

The Power Macintosh G3 computer incorporates several changes from earlier models. This section describes key issues you should be aware of to ensure that your hardware and software work properly.

System Software

The Power Macintosh G3 computer has a new system software architecture, called NewWorld, that provides Open Firmware booting and Mac OS Toolbox ROM in RAM. Mac OS 8.5 system software is installed on the startup drive. For more information, see Chapter 5, “System Software.”

DMA Addresses and NewWorld Software

In the past, Macintosh computers that use the PCI bus had a one-to-one correspondence between physical addresses and logical addresses as long as VM was off. To allow DMA transfers with VM on, DMA device drivers made a call to the `PrepareMemoryForIO` function to set up physical and logical mapping for their memory buffers. On Macintosh computers that use the NewWorld software, DMA device drivers must always make that call, whether VM is on or off. Information about how to use the `PrepareMemoryForIO` function appears on pages 219–229 of *Designing PCI Cards and Drivers for the Power Macintosh*.

Machine Identification and NewWorld Software

The Power Macintosh G3 described in this note and other Macintosh computers that implement the NewWorld software architecture no longer have unique machine ID values. Applications cannot determine which computer they are running on by reading the Gestalt Manager `gestaltMachineType` values. If an application requires a name string value for the computer model, the application should instead check the name registry for the value of the

"Devices:device-tree:model" property to get a name string for the machine. The current model property string is "PowerMac1,1".

No Graphics Support on MLB

The logic board in the Power Macintosh G3 computer does not include a built-in port for graphics output to an external monitor. Graphics output for the Power Macintosh G3 computer requires a PCI graphics card. A 2D/3D accelerated graphics card designed for the Power Macintosh G3 computer is installed in the 66 MHz PCI slot to support graphics output. For information about video monitors and the graphics card, see “Video Monitor Port” (page 55).

No Built-in AV I/O Connectors

Composite video and S-Video connectors are not available on the Power Macintosh G3 computer. Digital video input and output features of the Power Macintosh G3 computer are provided by the FireWire ports and the built-in USB ports. The USB ports have a maximum speed of 12 Mbits per second and may not be suitable for video output to high-speed external storage devices.

The Power Macintosh G3 computer does not include RCA jacks for analog stereo audio input and output. The built-in 3.5 mm sound input and sound output connectors can be used for analog stereo audio input and output. Digital audio input and output associated with digital video are supported by the FireWire interface; see “FireWire Ports” (page 48).

Modem Slot

The 70-pin modem connector in the Power Macintosh G3 computer is not the same as the connector on the modem slot in the original Power Macintosh G3 computers. The modem slot is strictly for Apple-designed modem cards.

PCI Expansion Slots

The Power Macintosh G3 computer includes four PCI expansion slots. Three of the slots, slots B, C, and D (2, 3, and 4), are 5 V, 64-bit, 33 MHz slots that support both 32-bit and 64-bit PCI cards that are compliant with the PCI V2.1

specification. The other slot, slot A (1), is a 3.3 V, 32-bit, 66 MHz slot dedicated to a 2D / 3D accelerated graphics card.

The 66 MHz PCI slot conforms to the PCI V2.1 specification with the exception that its clock speed is fixed at 66 MHz, so it does not accept 33 MHz cards. The 66 MHz PCI slot is keyed for 3.3 V only operation. Older 5 V cards cannot be installed in the 66 MHz PCI slot.

For more information, see "PCI Expansion Slots" beginning on page 66.

Internal Storage Devices

Standard configurations of the Power Macintosh G3 computer include two unused drive bays in the bottom of the enclosure. The factory installed drive is located in the back bay (bay 3). Bays are numbered 1 through 3 from front to back, as shown in Figure 1-4.

The drive bays accommodate 1-inch-high 3.5-inch devices. A PCI controller card is required for adding internal or external storage devices in addition to those in the three drive bays. For more information, see "Disk Drives" beginning on page 51.

RAM Expansion

The logic board uses JEDEC-standard SDRAM DIMM cards that are 64-bit bus, nonparity, 168-pin, 3.3-volt, unbuffered, and PC-100 compliant. The speed of the devices must be 125 MHz (8 ns).

IMPORTANT

DIMMs with any of the following features are not supported in the Power Macintosh G3 computer: registers or buffers, PLLs, ECC, parity, or EDO RAM. ▲

The maximum supported height of SDRAM DIMM cards is 2 inches. The maximum number of devices supported on a DIMM is 16 SDRAM devices. For information about SDRAM DIMM configurations, see "RAM DIMMs" (page 64).

No L2 Cache Expansion

The backside L2 cache is integrated into the design of the microprocessor module. No cache expansion is possible without replacing the entire module.

ATA-3 Drives

The CD-ROM, DVD-ROM, and ZIP drives are ATAPI devices, rather than SCSI devices. They are connected to the ATA-3 channel on the main logic board. The ATA Manager software supports PIO Mode 4 and DMA Mode 2 data transfers for devices on the ATA-3 channel.

No SCSI Ports

The Power Macintosh G3 computer does not include built-in internal or external SCSI device connectors. Adding an internal or external SCSI device requires the use of a SCSI PCI card. Ultra2 SCSI (LVD) devices and PCI controller cards are standard in some configurations and are available as options at the time of purchase.

Line Voltages

The power supply is not self-configuring for different input voltages. The voltage switch is delivered preconfigured for the input voltage of the region in which the unit is originally purchased. If the computer is moved to another location where the input voltage is different, a voltage switch must be adjusted to accommodate the voltage change. The switch has two positions that support voltage ranges of 90 to 132 V or 180 to 264V.

Monitor Power

The monitor power socket is not switched. Any time power is connected to the power supply, power is available on the monitor power socket. A monitor that does not support energy-saving features that is connected to the monitor power socket does not power off when the computer is shut down. Monitors that do not support energy-saving features have to be switched manually.

No Video RAM Expansion

The Power Macintosh G3 computer does not include built-in video RAM nor a slot for video RAM expansion on the main logic board. The accelerated graphics card that is installed in the computer includes 16 MB of SDRAM video memory and does not support video RAM expansion.

No LocalTalk Serial Ports

The Power Macintosh G3 computer does not include RS-422 LocalTalk serial ports found on earlier Macintosh models. Serial I/O for external USB devices is provided by two USB ports. USB adapters are available from third parties to support Macintosh-compatible legacy serial devices.

USB Ports and Devices

The USB ports take the place of the serial I/O ports found on earlier Macintosh computers. Software shims have been implemented in the system software to allow existing applications that use ADB devices to work with USB devices.

The Power Macintosh G3 computer uses a USB keyboard and mouse similar to the USB keyboard and mouse introduced with the iMac computer.

USB game controllers are supported by the InputSprocket component of the Apple Games Sprockets software architecture. InputSprocket software and information about the InputSprocket APIs can be found at

http://developer.apple.com/dev/games/

CHAPTER 2

Architecture

This chapter describes the architecture of the main logic board and graphics expansion card. It describes the major components of the main logic board: the microprocessor and core ICs. Input and output connectors are discussed in Chapter 3, “I/O Features.”

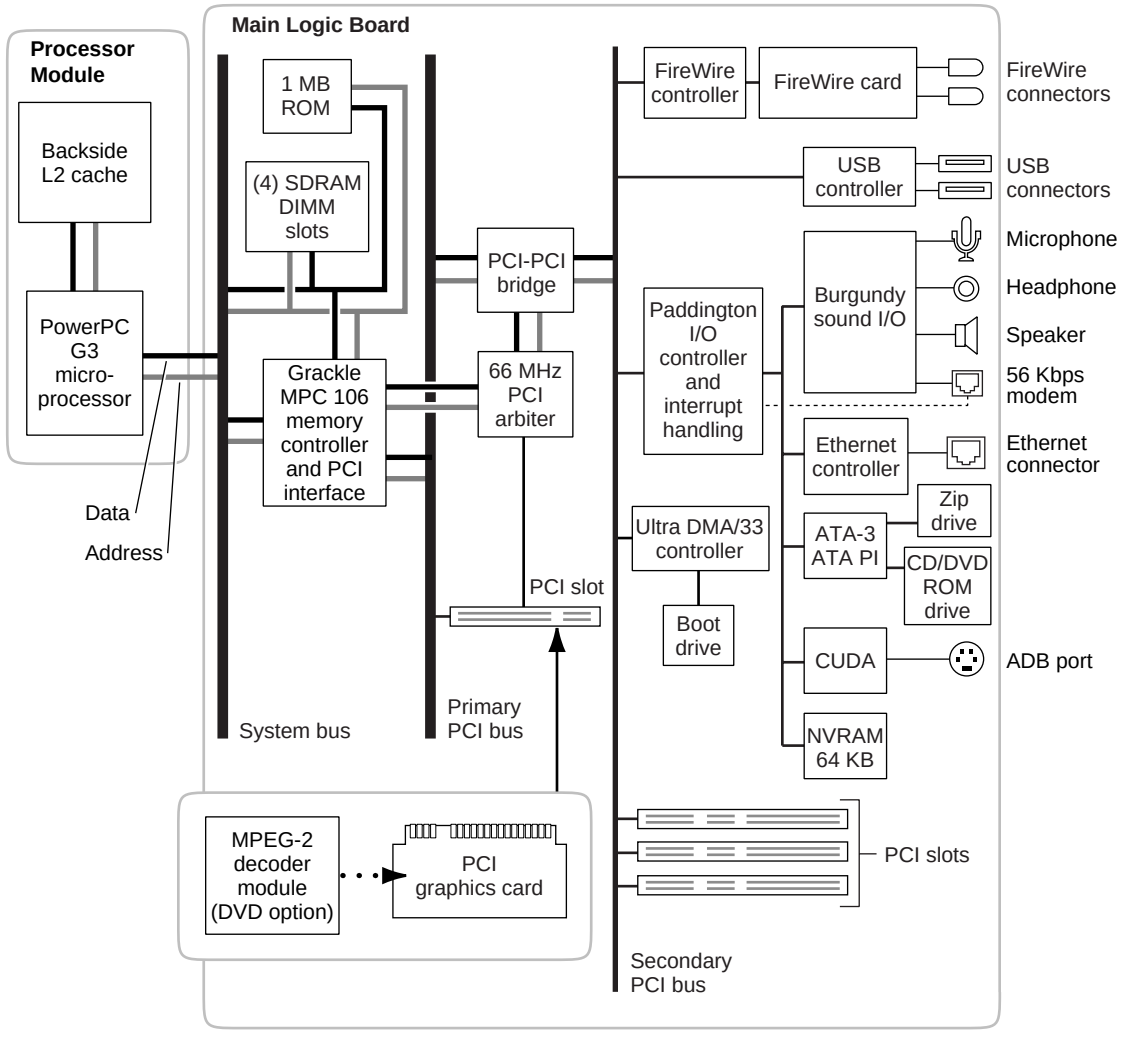
Block Diagram and Buses

The architecture of the main logic board is based on the PowerPC G3 microprocessor and three buses: the processor bus and two PCI buses, a primary 32-bit 66 MHz bus and a secondary 64-bit 33 MHz bus. The processor bus connects the microprocessor, cache, and main memory; the primary PCI bus is for an Apple graphics card solution; the secondary PCI bus connects the I/O devices. The I/O devices on the secondary PCI bus are

- Ultra DMA/33 (ATA-4) disk interface
- USB interface
- FireWire interface
- Paddington I/O controller IC
- PCI 33.33 MHz 64-bit slots B (2), C (3), and D (4)
- DEC/Intel 21154 PCI-PCI bridge IC

Figure 2-1 shows the main logic board block diagram.

Figure 2-1 Main logic board block diagram



Main Components

The following sections describe the principal electronic components on the computer's main logic board.

PowerPC G3 Microprocessor

The processor in the Power Macintosh G3 computer is a PowerPC 750 microprocessor running at 300 MHz, 350 MHz, or 400 MHz. Apple refers to these processors as PowerPC G3 microprocessors (G3 stands for "generation three").

The principal features of the PowerPC G3 microprocessor include

- full RISC processing architecture
- parallel processing units: load-store unit, two integer units, one complex integer unit, and one floating-point unit
- a branch manager that can usually implement branches by reloading the incoming instruction queue without using any processing time
- integrated L2 cache controller and Tag RAMs for high-performance memory access
- an internal memory management unit (MMU)
- 64 KB of on-chip cache memory (32 KB each for data and instructions)

For complete technical details, see the PowerPC Web pages at <http://www.mot.com/SPS/PowerPC/index.html> and <http://www.chips.ibm.com/products/ppc/overview/>.

The PowerPC G3 is located on a plug-in microprocessor card that includes the L2 cache.

Memory Subsystem

The memory subsystem consists of RAM and ROM on the main logic board as well as the backside second-level (L2) cache, which is located on a separate card

along with the microprocessor. The memory controller is described in “Grackle Memory Controller and PCI Bridge IC” (page 36).

Second-Level Cache

The backside second-level (L2) cache consists of 512 KB or 1 MB of SRAM. The cache is on the microprocessor card. The clock frequency of the cache is programmable and runs at one half the speed of the microprocessor, a ratio of 2:1. The L2 cache clock frequency can be divided down by 1, 1.5, 2, 2.5, or 3 from the core operating frequency of the PowerPC G3 microprocessor.

System ROM

With the NewWorld architecture, the system ROM consists of 1 MB of on-board ROM. It contains only the hardware specific code and tables needed to start up the computer, to load an operating system, and to provide common hardware access services. All the rest of the operaing system components that were formerly in ROM are now loaded from the boot device into RAM during the startup process. For a description of the ROM in the NewWorld architecture, refer to “Boot ROM Contents” (page 74).

System RAM

Four DIMM sockets are used for main memory. The DIMM sockets support SDRAM devices on 168-pin JEDEC-standard 3.3-volt unbuffered PC-100 SDRAM DIMMs. Supported DIMM sizes are 8, 16, 32, 64, 128, and 256 MB. The Grackle IC provides memory control for the system RAM. For more information, see “RAM DIMMs” (page 64).

Core ICs

The architecture of the main logic board is designed around five integrated circuits:

- the Grackle (MPC 106 v4) memory controller and PCI bus bridge
- DEC / Intel 21154 PCI-PCI bus bridge
- the Paddington I / O subsystem and DMA controller
- the Burgundy sound processor
- the Cuda soft-power controller

- the ATI 3D RAGE 128 GL video subsystem (on the accelerated graphics card)

The computer also uses several standard ICs for I/O support, which include the Ultra DMA/33 controller, the FireWire controller, and the USB controller. This section describes only the core ICs.

Grackle Memory Controller and PCI Bridge IC

The Grackle IC functions as the bridge between the PowerPC microprocessor bus and the I/O and graphics devices on the PCI buses. It provides buffering and address translation from one bus to the other.

The Grackle IC also provides the control and timing signals for ROM and RAM. The memory control logic supports byte, word, longword, and burst accesses to the system memory. If an access is not aligned to the appropriate address boundary, Grackle generates multiple data transfers on the bus.

Memory Control

The Grackle IC controls the system RAM and ROM and provides address multiplexing and refresh signals for the DRAM devices. For information about address multiplexing, see “RAM Address Multiplexing” (page 65).

PCI Bus Bridges

The Grackle IC acts as a bridge between the processor bus and the PCI expansion buses, converting signals on the PCI bus to the equivalent signals on the processor bus and vice-versa. The PCI bridge functions are performed by two converters. One accepts requests from the processor bus and presents them to the PCI bus. The other converter accepts requests from the PCI bus and provides access to the RAM and ROM on the processor bus.

The PCI bus bridge in the Grackle IC runs synchronously. The processor bus operates at a clock rate of 100 MHz, the primary PCI bus operates at 66.67 MHz and the secondary PCI bus at 33.33 MHz. A Dec/Intel 21154 PCI-to-PCI bus bridge IC synchronizes transactions on the primary and secondary PCI buses for the Grackle IC. Primary PCI bus arbitration is performed by the Apple Gated Clocks II IC. The PCI-to-PCI bridge IC performs arbitration services for the secondary PCI bus.

The PCI bus bridge generates PCI parity as required by the PCI bus specification, but it does not check parity or respond to the parity error signal.

Paddington I/O Controller IC

The Paddington IC is an enhanced I/O controller and DMA engine for Power Macintosh computers using the PCI bus architecture. The Paddington IC in the Power Macintosh G3 is an improved version of the Paddington IC used in the iMac computer. The primary change is improved performance with 100 Mbps Ethernet. The changes are for internal operation and are transparent to software.

Paddington also provides power-management control functions for energy saving features included on Power Macintosh computers. The Paddington IC is connected to the secondary PCI bus and uses the 33 MHz PCI bus clock.

The Paddington IC includes circuitry equivalent to the Ethernet, ATA-3, SCC, and VIA controller ICs. The functional blocks in the Paddington IC include the following:

- systemwide interrupt handling
- ATA-3 interface controller
- sound control logic and buffers
- 10/100 twisted-pair Ethernet controller

The Paddington IC provides bus interfaces for the following I/O devices:

- 56K modem card
- VIA system interface to the Cuda IC
- Burgundy sound input and output IC
- 64 KB nonvolatile RAM control

The Paddington IC also contains a serial interface and sound control logic for the Burgundy sound IC. The optional 56 Kbps modem uses the serial interface.

Burgundy Sound IC

The Burgundy sound IC combines a 16-bit digital sound encoder and decoder (codec). The Burgundy IC has the following sound controller features:

- Digitizes analog inputs with internal analog to digital converters (A/Ds).
- Creates analog outputs with internal digital to analog converters (DACs).
- Facilitates digital audio routing between the inputs and outputs and CPU.

- Provides digital gain, fade, balance, and mute controls.
- Provides digital tone control.

For additional information about the audio features, see “Sound System” (page 53).

Cuda IC

The Cuda IC provides several system functions, including

- management of soft system resets
- management of the real-time clock
- software control of the power supply
- I^2C bus control for Cuda (master), four DIMM slots, and clock buffer

Graphics Controller IC

The ATI 3D RAGE 128 GL graphics controller IC on the accelerated graphics card contains the logic for the video display. The ATI 3D RAGE 128 GL graphics controller includes the following features:

- advanced 128-bit rendering engine
- architecture optimized to support high-speed SDRAM video memory
- display memory controller, built-in drawing coprocessor, video scaler, color space converter, clock generator, and true color palette video DAC (digital-to-analog converter)
- video CLUT (color lookup table)
- hardware graphics acceleration with a 16-bit Z-buffer
- accelerated QuickDraw 3D rendering up to six times that of software-only acceleration
- true color palette DAC supporting pixel clock rates to 200 MHz for 1600 by 1200 resolution at 90 Hz
- graphics and video line buffer for superior video scaling and playback quality
- hardware cursor up to 64 x 64 x 2
- DDC1 and DDC2B+ for plug-and-play monitor support

- graphics control accessible through the QuickDraw, QuickDraw 3D, QuickDraw 3D RAVE, and QuickTime APIs

A separate data bus handles data transfers between the ATI 3D RAGE 128 GL graphics controller and the display memory. The display memory data bus is 64 bits wide, and all data transfers consist of 64 bits at a time. The RAGE IC breaks each 64-bit data transfer into several pixels of the appropriate size for the current display mode—4, 8, 16, 24, or 32 bits per pixel.

The ATI 3D RAGE 128 GL graphics controller IC uses several clocks. Its transactions are synchronized with the PCI bus. Data transfers from the frame-buffer RAM are clocked by the MEM_CLK signal. Data transfers to the CLUT and the video output are clocked by the dot clock, which has a different rate for different display monitors.

The 2D graphics accelerator is a fixed-function accelerator for rectangle fill, line draw, polygon fill, panning/scrolling, bit masking, monochrome expansion, and scissoring.

Display Memory

The display memory on the accelerated graphics card is separate from the main memory. The display memory consists of 16 MB of 100 MHz/10 ns SDRAM devices configured to make a 64-bit data bus. The display memory cannot be expanded.

With the 16 MB of video memory, the display data generated by the computer can have pixel depths of 8, 16, or 32 bits for monitors up to1920 by 1080 pixels. For a complete listing of the display resolutions, see “Display Resolution Modes” (page 59).

USB Controller

The USB controller is a standard USB controller IC with two USB connectors that support USB devices with data transfer rates of 1.5 Mbps or 12 Mbps. The register set complies with the Open Host Controller Interface (OHCI) specification.

FireWire Link Controller

The Texas Instruments PCI-Lynx FireWire controller IC supports the IEEE 1394 FireWire high-speed serial interface standard at 100, 200, and 400 Mbps. It provides the link interface layer to the FireWire physical layer on the FireWire card.

Optional Internal Modem

The optional internal hardware modem is a separate module that is connected to the SCC port A of the Paddington IC. The module contains a modem controller IC, a data pump, and the interface to the telephone line (DAA).

USB Compatibility Issues

The USB ports augment the ADB ports and take the place of the serial I/O ports found on earlier Macintosh computers, but they do not function the same way. The following sections describe the differences.

ADB Compatibility

Apple is providing an ADB/USB shim to support processes that control ADB devices by making calls to the ADB Manager and the Cursor Device Manager. The ADB/USB shim makes it possible for processes that support an ADB keyboard to work with the USB keyboard equivalent.

For example, the ADB/USB shim allows applications to set the Caps Lock and Num Lock LEDs on the Apple USB keyboard. The ADB/USB shim also allows the Cursor Device Manager to support a USB mouse.

Keyboards other than the Apple USB keyboard can be used with the Power Macintosh G3 computer, but they will be treated as having an ADB device ID of 2.

IMPORTANT
The ADB/USB shim does not support USB devices other than the keyboard and mouse. s

Note
The ADB/USB shim is built into the Mac OS ROM image on the Power Macintosh G3 computer, as it is on all Power Macintosh systems that have USB ports. u

Serial Port Compatibility

The Þrst release of the Mac OS USB DDK does not include a universal Serial/USB shim that would allow processes that use the Communications ToolboxÕs Communications Resource Manager (CRM) to Þnd and use a USB modem device. Any USB modem device would need to implement its own communication shim to provide an interface between the CRM and its USB Communication class driver.

For more information, please refer to the Mac OS USB DDK, which is available from the Apple Developer DDK page on the World Wide Web, at

http://developer.apple.com/sdk/

▲ **WARNING**
A bus-powered hub as defined in the USB specification does not provide enough power to support a second bus-powered hub. A second bus-powered hub must be connected to the second USB port on the computer, not to a port on the Apple USB keyboard. ▲

Apple provides a HID class driver for the Apple USB keyboard, which supports the USB boot protocol. Other keyboards intended for use on the Macintosh platform must support the HID boot protocol, as defined in the USB Device Class Definition for Human Interface Devices (HIDs).

Mouse

The Apple USB mouse is designed to work with the computer by way of the USB ports. The mouse case is round and has the same two-tone color design as the case of the computer. The Apple USB mouse operates as a low-speed (1.5 Mbps) USB device.

The mechanism inside the Apple USB mouse is similar to that in the Apple Desktop Bus Mouse II. The mouse ball is removeable for cleaning; the ring that allows access to the ball can be locked by inserting an unfolded paper clip into a small hole and turning the ring clockwise.

FireWire Ports

The computer includes two external FireWire IEEE 1394 ports on the rear panel of the enclosure. The features of the FireWire ports are:

- support high-speed serial I/O at 100, 200, and 400 Mbps
- provide 15 watts of power when the computer system is on
- accept external power input on FireWire bus when system is off

The FireWire hardware and software provided with the computer are capable of all asynchronous and isochronous transfers defined by IEEE standard 1394-1995. Developers of FireWire peripherals are required to provide device drivers.

It is possible to connect two computers to each other using a FireWire cable, but no software is provided to make use of such a connection. Also, third-party software such as video editing applications may not deal gracefully with a shared FireWire peripheral if two or more computers attempt to communicate with it at the same time.

FireWire Connector

The FireWire connector has six contacts, as shown in Figure 3-3. The connector pin assignments are shown in Table 3-3.

Figure 3-3 FireWire connector

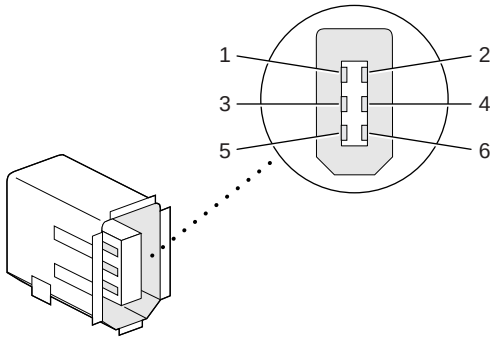


Table 3-3 FireWire connector pin assignments

Pin	Signal name	Description
1	Power	Unregulated DC; 24 V no load
2	Ground	Ground return for power and inner cable shield
3	TPB-	Twisted-pair B, differential signals
4	TPB+	
5	TPA-	Twisted-pair A, differential signals
6	TPA+	
Shell	—	Outer cable shield

The power pin provides a maximum voltage of 24 V (no load) and up to 15 W total power on both connectors. When the computer is off, the power pin accepts external power at 8 to 33 V, in conformity with the P1394a draft standard.

Pin 2 of the 6-pin FireWire connector is ground for both power and inner cable shield. If a 4-pin connector is used on the other end of the FireWire cable, its shell should be connected to the wire from pin 2.

The signal pairs are crossed in the cable itself so that pins 5 and 6 at one end of the cable connect with pins 3 and 4 at the other end. When transmitting, pins 3 and 4 carry data and pins 5 and 6 carry clock; when receiving, the reverse is true.

For additional information about the FireWire interface and the Apple APIs for FireWire device control, refer to the resources available on the Apple FireWire Web site at

http://devworld.apple.com/dev/FireWire/index.html

or send electronic mail to

firewire@apple.com

Ethernet Port

The Power Macintosh G3 computer has a built-in 10/100 Mbps Ethernet port. The user can connect it to either a 10Base-T or a 100Base-TX hub; the port automatically senses which type of hub is connected.

The connector for the Ethernet port is an RJ-45 connector on the back of the computer.

The Ethernet interface in the Power Macintosh G3 computer conforms to the ISO/IEC 802.3 specification, where applicable.

Internal Modem

The Power Macintosh G3 computer includes an option for an internal modem. The modem interface to the main logic board is a 70-pin connector. The external

I/O connector for the modem is an RJ-11 connector located on the back of the computer. The modem has the following features:

- modem bit rates up to 56 Kbps (supports K56flex, V.34, and V.90 protocols)
- fax modem bit rates up to 14.4 Kbps

The modem appears to the system as a serial port that responds to the typical AT commands. The modem provides a sound output for monitoring the progress of the modem connection.

Note
This developer note does not provide the electrical or mechanical specifications for the 70-pin modem interface to the main logic board.

Disk Drives

The Power Macintosh G3 computer has an Ultra DMA/33 (ATA/ATAPI-4) interface and an ATA-3 interface for internal mass storage and removable media devices. The enclosure includes data and power connectors for the boot drive on the Ultra DMA/33 interface. It also includes data and power connectors for an optional internal ATAPI CD-ROM or DVD-ROM drive and an internal ATAPI ZIP drive. Those drives are connected to the ATA-3 interface.

The enclosure also includes two additional drive bays for other mass storage devices connected to an optional or user-installed controller card in a PCI slot. None of the drive bays can be modified to support removable drive bay kits. The locations of the drive bays are shown in Figure 1-4.

The Ultra DMA/33 bus supports PIO Mode 4, DMA Mode 2, and Ultra DMA Mode 2 data transfers. The ATA-3 bus supports PIO Mode 4 and DMA Mode 2 data transfers.

The ATA-3 channel supports two ATA devices. The devices are configured in a ATA Device 0/1 configuration. The ATAPI CD or DVD-ROM and Zip drive, when installed, occupy both device locations on the ATA-3 channel. The ATAPI CD or DVD-ROM, depending on which is installed, is Device 0 (master), and the Zip drive is Device 1 (slave). If the Zip drive is not factory installed in the system, a power and data cable is available for adding a Zip drive to the ATA-3

bus in the Zip drive bay. The device has to be device-select jumpered as Device 1 (slave).

The Power Macintosh G3 computer does not include a 1.44 MB floppy drive.

Ultra DMA/33 Hard Disk Drive

The logic board supports an internal hard disk drive that uses the Ultra DMA / 33 (ATA / ATAPI-4) interface. The Power Macintosh G3 comes with an Ultra DMA / 33 hard disk or an Ultra2 SCSI hard disk installed in Slot 3.

The internal hard disk drive has a 40-pin connector and a separate 4-pin power connector. An 80-conductor high-density cable with a 40-pin connector is attached to the main logic board. To provide improved signal quality, the 80-conductor cable provides a separate ground for each of the signals on the 40 pin connector. The separate power cable is attached directly to the power supply.

Optional Ultra2 SCSI (LVD) Drive

An optional Ultra2 SCSI (LVD) disk drive and Ultra2 SCSI (LVD) PCI controller card are available as a configuration option. The Ultra2 SCSI (LVD) interface provides data transfer rates of up to 80 MB per second. Additional information about the Ultra2 SCSI (LVD) interface can be found at:

http: / / www.quantum.com / src / whitepapers /

ATAPI CD-ROM Drive

The Power Macintosh G3 computer has a 24x-speed internal ATAPI CD-ROM drive. The CD-ROM drive supports the worldwide standards and specifications for CD-ROM and CD-digital audio discs described in the Sony / Philips Yellow Book and Red Book. The drive can read CD-ROM, CD-ROM XA, CD-I, and PhotoCD discs as well as play standard audio discs.

The CD-ROM drive has a sliding tray to hold the disc. The drive features a mechanism that supports 4x, 8x, 12x, and 24x data transfer rates and a data buffer that further enhances performance. The CD is connected as device 0 in a ATA Device 0 / 1 configuration.

Optional ATAPI Zip Drive

The Zip drive is an ATAPI drive and is connected as device 1 in an ATA Device 0/1 configuration on the ATA-3 channel of the main logic board.

Optional DVD-ROM Drive

The optional DVD-ROM drive is fully compatible with existing CD-ROM media. The drive supports CD-ROM at 32x speed maximum and DVD at 5x constant linear velocity (CLV). The DVD-ROM drive supports the following disc formats:

- DVD-ROM (One-layer or two-layer, one-sided or two-sided)
- CD-ROM (Modes 1 and 2), CD-ROM XA (Mode 2, Forms 1 and 2), CD-Audio, Photo CD, CD-RW, CD-R, CD-Extra
- CD-I (Mode 2, Forms 1 and 2), CD-I Ready, CD-I Bridge
- Video CD

Sound System

The sound system for the Power Macintosh G3 computer supports 44.1 kHz 16-bit stereo sound output and input, available simultaneously.

Like other AV class Macintosh computers, the sound circuitry and system software can create sounds digitally and either play the sounds through speaker inside the enclosure or send the sound signals out through the sound output jack. The Power Macintosh G3 computer also records sound from several sources: an analog sound source connected to the line-level sound input jack, analog sound from the modem card connected to the internal modem connector, or a compact disc in the CD-ROM player. With each sound input source, sound playthrough can be enabled or disabled.

Sound Outputs

The Power Macintosh G3 computer provides one 3.5-mm mini jack for sound output on the back of the enclosure.

The output jack is connected to the sound amplifier; the mini jack is intended for connecting a pair of headphones or amplified external speakers. Inserting a plug into the sound output mini jack disconnects the built-in speaker. The computer has one built-in speaker.

The Burgundy IC provides the stereo sound output to both the internal speakers and the sound output jack.

The sound output jack has the following electrical characteristics:

- output sound signal to noise ratio (SNR) <90 dB unweighted (typical) when sound playback is from system hard disk drive or main memory
- output sound SNR <80 dB unweighted (nominal) when playback is from CD
- overall output sound SNR <90 dB unweighted (typical)

Sound Inputs

The Power Macintosh G3 computer provides a stereo sound input jack on the back of the enclosure for connecting an external PlainTalk microphone or other sound source. The sound input jack accepts a standard 3.5-mm stereophonic phone plug (two signals plus ground).

Note
The Apple PlainTalk microphone requires power from the main computer, which it obtains by way of an extra-long, 4-conductor plug that makes contact with a 5-volt pin inside the sound input jack. ◆

The sound input jack has the following electrical characteristics:

- input impedance: 20 kΩ
- maximum input level without distortion: 2.5 V peak to peak (Vpp) maximum
- line-level microphone voltage range of 0.28 V to 2.1 V peak to peak
- input SNR <90 dB unweighted (typical) for recording to system hard disk drive or main memory

Digitizing Sound

The sound circuitry digitizes and records sound as 44.1 kHz 16-bit samples. If a sound sampled at a lower rate on another computer is played as output, the

Sound Manager transparently upsamples the sound to 44.1 kHz prior to outputting the audio to the Burgundy sound IC.

When recording sound from a microphone, applications that are concerned about feedback should disable sound playthrough by calling the Sound Manager APIs.

The Burgundy IC provides separate sound buffers for input and for stereo output so that the computer can record and send digitized sound to the sound outputs simultaneously.

Video Monitor Port

The Power Macintosh G3 computer has a built-in accelerated graphics card that provides the port for the external video monitor.

Graphics Card

The accelerated graphics card in the Power Macintosh G3 computer has the following features:

- 128-bit 2D/3D graphics and multimedia accelerator IC, the ATI 3D RAGE 128 GL
- 16 MB of synchronous dynamic RAM (SDRAM) soldered to the card (no video RAM expansion)
- hardware acceleration of 2D QuickDraw graphics and video to speed up scrolling text and graphics and screen redraw operations
- hardware acceleration of video for full screen, full motion, TV-quality playback of Cinepak and MPEG1 QuickTime movies
- connector for the DVD decode module supporting the playback of DVD video
- bilinear hardware interpolation and scaling
- accelerated 3D QuickDraw rendering up to six times that of software-only rendering
- real-time 3D shaded object manipulation, animation, and virtual world navigation

- 16-bit Z buffer for hidden texture surface removal
- six perspectively correct texture mapping functions
- alpha blending, transparency, and fog effects
- flat and Gouraud shading
- video textures and video lighting

The graphics acceleration features enhance the realism of 3D interactive application software and games.

Monitor Connector

The monitor connector is a standard DB9/15 (also called mini sub D15) connector for use with a VGA, SVGA, or XGA monitor. Figure 3-4 shows the pin configuration and Table 3-4 lists the signal pin assignments.

Figure 3-4 Monitor connector

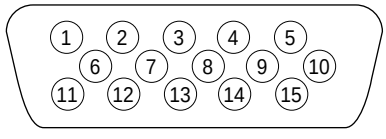


Table 3-4 Monitor connector pin assignments

Pin	Signal name	Description
1	RED	Red video signal
2	GREEN	Green video signal
3	BLUE	Blue video signal
4	MONID(0)	Monitor ID signal 0
5	GND	DDC return
6, 7, 8	AGND_VID	Analog video ground
9	+5V_IO	5 V power for I/O device

Table 3-4 Monitor connector pin assignments (continued)

Pin	Signal name	Description
10	GND	HSYNC and VSYNC ground
11	VGA_ID	VGA ID signal
12	MONID(2)	Monitor ID signal 2
13	HSYNC	Horizontal synchronization signal
14	VSYNC	Vertical synchronization signal
15	MONID(1)	Monitor ID signal 1

Monitor Adapter

An monitor adapter (included with the computer) allows the user to connect a standard Apple monitor cable to the computer. The adapter enables the computer to recognize a wide range of monitor types. The Apple part number for the adapter is 590-1120.

Monitor Sense Codes

To identify the type of monitor connected, the computer first determines whether the adapter is connected. It does this by checking pin 11; on the new adapter, this pin is connected to the VSYNC signal. If the adapter is not found, the computer next checks to determine whether a DDC-type monitor is connected. DDC is the interface that provides monitor ID signals for VGA and SVGA monitors.

If the computer does not detect a DDC-capable monitor, it uses the Apple monitor sense codes on the signals MONID(0–2) in Table 3-4. Table 3-5 shows the sense codes and the extended sense codes for each of the monitors the card can support.

Note
The Apple Studio Display 17" / viewable 16" is listed in Table 3-5 with sense code value $06-23, but it is identified using DDC on most Macintosh computers. ◆

Table 3-5 Monitor sense codes

Monitor type	Standard sense code	Extended sense code		
	(S2–0)	(S1,0)	(S2,0)	(S2,1)
Macintosh 21-inch Color Display	0 0 0	—	—	—
Macintosh Portrait Display	0 0 1	—	—	—
Macintosh 12-inch RGB Display	0 1 0	—	—	—
Apple Two-Page Monochrome Monitor	0 1 1	—	—	—
NTSC monitor	1 0 0	—	—	—
15-inch RGB monitor	1 0 1	—	—	—
Apple Multiple Scan 14 or 15 Display	1 1 0	0 0	0 0	1 1
Apple Multiple Scan 17 or 1705 Display	1 1 0	0 0	1 0	1 1
Apple Studio Display 17" / viewable 16" or Apple Multiple Scan 20 Display	1 1 0	1 0	0 0	1 1
Apple Studio Display 15", AppleStudio Display 21" with Colorsynch technology, AppleVision 850, 850av, 1710, and 1710av Displays, Macintosh 12-inch Monochrome Display, or AppleColor High Resolution RGB Monitor	1 1 0	1 0	1 0	1 1
PAL monitor	1 1 1	0 0	0 0	0 0
NTSC monitor, with convolution	1 1 1	0 1	0 1	0 0
VGA or SVGA monitor	1 1 1	0 1	0 1	1 1
Macintosh 16-inch Color Display	1 1 1	1 0	1 1	0 1
PAL monitor, with convolution	1 1 1	1 1	0 0	0 0
19-inch RGB monitor	1 1 1	1 1	1 0	1 0
No monitor connected	1 1 1	1 1	1 1	1 1

For a complete description of the sense code system, refer to Technote HW 30 *Sense Lines*. To find out how to obtain Apple Technical Notes, see “Supplemental Reference Documents” (page 12).

Display Resolution Modes

When power is applied, the monitor is initially set for a display size of 640 by 480 pixels. With a multisync monitor the user can switch the monitor resolution on the fly by using the BitDepths and Resolutions modules in the control strip or the Monitors & Sound control panel.

Table 3-6 shows the display resolution, vertical and horizontal scan rates, and maximum pixel depths supported by the accelerated graphics card with the ATI 3D RAGE 128 GL graphics controller. The 16 MB of video RAM on the accelerated graphics card supports pixel depths up to 32 bits per pixel at all resolutions.

Table 3-6 Supported display resolutions

Display resolution	Vertical scan rate	Horizontal scan rate
512 by 384	70 Hz	31.488 kHz
640 by 480	60 Hz	31.469 kHz
640 by 480	67 Hz	35.00 kHz
640 by 480	72 Hz	37.861 kHz
640 by 480	75 Hz	37.500 kHz
640 by 480	85 Hz	43.269 kHz
640 by 870	75 Hz	68.85 kHz
800 by 600	56 Hz	35.156 kHz
800 by 600	60 Hz	37.879 kHz
800 by 600	72 Hz	48.077 kHz
800 by 600	75 Hz	46.875 kHz
800 by 600	85 Hz	53.674 kHz
832 by 624	74.5 Hz	49.725 kHz
1024 by 768	60 Hz	48.363 kHz
1024 by 768	70 Hz	56.476 kHz

Table 3-6 Supported display resolutions (continued)

Display resolution	Vertical scan rate	Horizontal scan rate
1024 by 768 (VESA)	75 Hz	60.023 kHz
1024 by 768 (19” RGB)	75 Hz	60.241 kHz
1024 by 768	85 Hz	68.677 kHz
1152 by 870	75 Hz	68.681 kHz
1280 by 960	75 Hz	75.000 kHz
1280 by 1024	60 Hz	63.981 kHz
1280 by 1024	75 Hz	79.976 kHz
1280 by 1024	85 Hz	91.146 kHz
1600 by 1200	60 Hz	75 kHz
1600 by 1200	65 Hz	81.250 kHz
1600 by 1200	70 Hz	87.500 kHz
1600 by 1200	75 Hz	93.750 kHz
1920 by 1080	60 Hz	70.313 kHz
1920 by 1080	71 Hz	84.375 kHz

Graphics Acceleration Display Modes

Table 3-7 shows the display modes for QuickDraw 3D acceleration. (QuickDraw 2D acceleration is supported in all modes.)

Table 3-7 Supported graphics acceleration display modes

Display resolution	Pixel depth	Vertical scan rates	QuickDraw 3D acceleration
512 by 384	8	70 Hz	No
512 by 384	16, 32	70 Hz	Yes
640 by 480	8	60 Hz, 67 Hz, 72 Hz, 75 Hz, 85 Hz	No
640 by 480	16	60 Hz, 67 Hz, 72 Hz, 75 Hz, 85 Hz	Yes
640 by 480	32	60 Hz, 67 Hz, 72 Hz, 75 Hz, 85 Hz	Depends on application's window size
640 by 870	16	75 Hz	No
800 by 600	8, 32	56 Hz, 60 Hz, 72 Hz, 75 Hz, 85 Hz	No
800 by 600	16	56 Hz, 60 Hz, 72 Hz, 75 Hz, 85 Hz	Depends on application's window size
832 by 624	8, 32	75 Hz	No
832 by 624	16	75 Hz	Depends on application's window size
1024 by 768	8, 16	60 Hz, 70 Hz, 75 Hz	No
1152 by 870	16	75 Hz	No
1280 by 980	8	75 Hz	No
1280 by 1024	8	60 Hz, 75 Hz	No

CHAPTER 4

Expansion Features

This chapter describes the expansion features of the logic board: the RAM expansion slot, the video RAM, and the PCI expansion slots.

RAM DIMMs

The logic board has four 168-pin RAM expansion slots. At least one of the RAM expansion slots contains a factory installed SDRAM DIMM.

The RAM expansion slots accept SDRAM DIMMs that are 3.3 volt, unbuffered, 8-byte, non-parity, and PC-100 compliant. The speed of the SDRAM devices must be rated at 125 MHz (8 ns) or faster.

IMPORTANT
DIMMs with any of the following features are not supported in the Power Macintosh G3 computer: registers or buffers, PLLs, ECC, parity, or EDO RAM. ▲

The 8-byte, 168-pin DIMM has one 64-bit-wide data bus per bank.

The minimum bank size supported by the Grackle memory controller IC is 2 MB, and the largest is 128 MB. The largest DIMM supported is a two-bank DIMM of 256 MB using 128 Mbit SDRAM devices. The maximum number of devices per DIMM is 16.

The SDRAM DIMMs can be installed one or more at a time. The logic board supports linear memory organization; no performance gains are seen when two DIMMs of the same size are installed. Any supported size DIMM can be installed in any DIMM slot, and the combined memory of all of the DIMMs installed is configured as a contiguous array of memory.

Mechanical Specifications

The mechanical design of the SDRAM DIMM is defined by the JEDEC MO-161 specification. The specification can be found on the world-wide web at

http://www.jedec.org/download/freestd/pub95/mo161C.pdf

The maximum height of DIMMs for use in the Power Macintosh G3 is 2.00 inches.

Presence Detect EEPROM

The presence detect serial EEPROM specified in the JEDEC standard is required and must be set to properly define the DIMM configuration. Details about the required values for each byte on presence detect EEPROM can be found in sections 4.5.4 and 4.1.2.5 of the JEDEC standard 21-C, release 7 specification.

RAM Address Multiplexing

Signals A[0–13] on each SDRAM DIMM make up a 14-bit multiplexed address bus that can support several different sizes of SDRAM devices. Table 4-1 shows the address multiplexing modes used with the devices. The devices are characterized by their bit dimensions: for example, a 1 M by 16-bit device addresses 1 M and stores 16 bits at a time.

Table 4-1 Address multiplexing modes for SDRAM DIMMs

Device size	Device configuration	Size of row address	Size of column address
16 Mbits	2 M x 4 x 2	11	10
16 Mbits	1 M x 8 x 2	11	9
16 Mbits	512K x 16 x 2	11	8
64 Mbits	8 M x 4 x 2	13	10
64 Mbits	4 M x 4 x 4	12	10
64 Mbits	4 M x 8 x 2	13	9
64 Mbits	2 M x 8 x 4	12	9
64 Mbits	2 M x 16 x 2	13	8
64 Mbits	1 M x 16 x 4	12	8
64 Mbits	1 M x 32 x 2	13	8
64 Mbits	512K x 32 x 4	12	8
128 Mbits	16 M x 8 x 2	13	10
128 Mbits	16 M x 8 x 4	12	10

Table 4-1 Address multiplexing modes for SDRAM DIMMs (continued)

Device size	Device configuration	Size of row address	Size of column address
128 Mbits	8 M x 16 x 2	13	9
128 Mbits	8 M x 16 x 4	12	9
128 Mbits	4M x 32 x 2	13	8
128 Mbits	4M x 32 x 4	12	8

SDRAM Devices

The memory controller in the Grackle IC supports 1 Mbit, 4 Mbit, 8 Mbit, 16 Mbit, 64 Mbit, and 128 Mbit SDRAM devices that are PC-100 compliant. The speed of the SDRAM devices should be rated at 125 MHz (8 ns) or faster. The Grackle memory controller IC is configured to detect devices with a CAS latency as low as 1 and as high as 3. The Grackle IC is configured to support the slowest SDRAM bank it detects in the system. The access time from clock at CAS latency of 3 should be 7 ns or faster. Burst length should be at least 4 and the minimum clock delay for back-to-back random column accesses should be a latency of 1 clock.

IMPORTANT

The DIMM modules used in any previous Power Macintosh or Power Macintosh G3 computer model are not compatible with the Power Macintosh G3 described in this note. The SDRAM DIMM modules must be PC-100 compliant, 168-pin, 3.3-volt, unbuffered, and rated at 125 MHz (8 ns) or faster.

PCI Expansion Slots

The logic board uses the industry-standard peripheral component interconnect (PCI) bus for an I/O expansion bus. The Power Macintosh G3 has a primary 66 MHz bus and a secondary 33 MHz PCI bus. The 66 MHz bus is a 32-bit multiplexed address and data bus. The 33 MHz bus is a 64-bit multiplexed address and data bus.

The primary PCI bus includes slot 1, which accommodates only 32-bit 66 MHz +3.3 V PCI cards. Slot 1 conforms to the PCI V2.1 specification with the exception that its clock speed is fixed at 66 MHz so it does not accept 33 MHz cards.

The Power Macintosh G3 computer is always configured with an Apple 2D/3D accelerated graphics card installed in slot 1, so that slot is not available for PCI card expansion unless the card is removed. Slot 1 is keyed for 3.3V only operation, so older 5V cards cannot be installed in that slot.

The secondary PCI bus includes slots 2, 3, and 4, which accommodate both 32-bit and 64-bit 33 MHz +5V PCI cards.

The logic board accepts standard 6.88-inch and 12.283-inch PCI cards as defined by the *PCI Local Bus Specification*, Revision 2.1. The cards are required to use the standard ISA fence described in the specification.

The PCI slots support all the required PCI signals and certain optional PCI signals. The three 33 MHz PCI slots on the logic board support the optional 64-bit bus extension signals and cache support signals.

For more information about the PCI expansion slot, refer to *Designing PCI Cards and Drivers for Power Macintosh Computers.*

The Modem Interface

The modem interface on the Power Macintosh G3 logic board is a 70-pin connector for an Apple 56 Kbps modem. The electrical and mechanical specifications for the modem connector are not provided in this developer note. Apple does not support third-party development of modems for this slot.

CHAPTER 5

System Software

The latest Power Macintosh G3 computer is different from previous Macintosh computers in that it has no single, large ROM that contains the many components of the Mac OS software, along with the 68K emulator, hardware initialization, and the nanokernel. Instead, a small ROM provides hardware initialization functions and provides a mechanism to load the Mac OS ROM image into RAM. The new software architecture that is centered around ROM-in-RAM and its ramifications has the code name NewWorld.

The New Approach

Historically, the Macintosh ROM has been structured as one monolithic ROM, known as the Mac OS ROM, that contains both low level and high level software. That is, the ROM contains the hardware-specific code needed by the computer at power-up time as well as higher level Mac OS software. Examples of hardware-specific code are drivers, feature tables, diagnostics, and hardware initialization code. Examples of higher level software are high-level managers, QuickDraw, SCSI Manager, and so on.

As features have been added to the Mac OS software, some of the higher level code expanded beyond the practical limits provided by ROMs, so the ROM has been augmented and modified by system software such as the System file and the hardware enabler. In this way the functionality of the ROM has been spread out among the ROM, the enabler, and disk-based system software. This intertwining of low-level and high-level code spread out from ROM to disk has made it difficult and time consuming to release new computers.

One way to address this problem is to separate the system software into two logically distinct pieces. One piece holds most of the hardware-specific components needed to boot the computer, while the other contains boot-time Mac OS routines and components that are common to many Macintosh models. With this approach, much of the hardware-specific code is isolated in the boot ROM, and the Mac OS and system software code can be made abstract and generic. This approach has several benefits.

- When hardware changes are needed, only the hardware-specific code in the boot ROM has to be modified, greatly decreasing turnaround time for new product releases and reducing testing time and expenses.

- The high-level Mac OS and system software does not need to change often. When making a new build as a result of changing hardware-dependent code, there is high confidence that the high-level software has not been changed.
- Not changing the higher level software as often simplifies things for many groups inside Apple, including testing, system software, software configuration management, developer support, and publications. Third-party developers can also benefit from this.

What Has Changed

Hardware-specific code that performs the computer's start-up activities resides in firmware (ROM). That code fits into one ROM called the boot ROM. The boot ROM includes the hardware specific code and tables needed to start up the computer, to load an operating system, and to provide common hardware access services.

All higher level software resides somewhere else. For now, think of it residing in what has been historically known as the Mac OS ROM, but with much of the old hardware-specific code moved into the boot ROM. As before, the Mac OS ROM can still be augmented by enablers, the System file, and extensions.

Prior to the iMac, all Macintosh computers required a ROM component that contained manyh components of the Mac OS software. The NewWorld approach sidesteps this requirement by copying an image of the Mac OS ROM into RAM before the Mac OS begins operation. The area of RAM that contains the Mac OS ROM image is excluded from the available memory space in RAM and is marked as read-only. Once the Mac OS begins operation, a Mac OS ROM image in RAM and an actual Mac OS ROM behave in the same way.

No new or different software interfaces are directly accessible from the Mac OS. During the boot process, software contained in the Mac OS ROM file communicates with Open Firmware to collect information about the hardware, using the Open Firmware Client Interface.

Note
Open Firmware is a central component of the NewWorld architecture. For information on how to get reference material about Open Firmware, see "Open Firmware" (page 13). ◆

Most of the changes are completely transparent to the Mac OS. Only the Startup Disk control panel is affected: it includes added code to modify the Open Firmware's configuration variables in the NV-RAM.

Features of the New Approach

Because the latest Power Macintosh G3 computer has new hardware features that are different from other Macintosh computers, new software features are needed in addition to the NewWorld requirements for other Macintosh computers. This list includes features that implement the NewWorld approach along with features that support the new hardware features:

- Power-on Self Test (POST) software, which resides in the boot ROM, provides hardware initialization and diagnostic functions.
- Open Firmware, which resides in ROM, completes hardware initialization, provides a description of the hardware, loads initial operating system software, and transfers control to that software.
- Run-Time Abstraction Services (RTAS), which resides in ROM, is instantiated into RAM through an Open Firmware method called by the OS. RTAS provides functions that are available to the operating system at any time to access platform-specific hardware, such as the real-time clock and NV-RAM.
- Mac OS ROM image, a file that contains the high-level software that resides in the Mac OS ROM on other Macintosh computers.
- 10Base-T / 100Base-TX Ethernet device driver, in the boot ROM.
- Device driver for the USB hub, Apple USB keyboard, and Apple USB mouse, in the Mac OS ROM image.

In addition to the above new features, changes have been made to the source base for the components of the Mac OS ROM to abstract it from the hardware. These changes are designed to reduce bring-up time and effort, improve reliability of the Mac OS ROM components, and reduce testing time by moving the changes necessary for a new computer to the boot ROM. Some of the hardware components accessed through this new abstracted software are the interrupt controller, ADB, USB, SCSI, ATA (IDE), sound, and Ethernet.

Performance

Performance of a Power Macintosh G3 computer using ROM in RAM should exceed performance measurements for other Macintosh computers with

comparable CPUs and speeds due to improved interrupt handling with the NewWorld approach. In addition, performance is improved due to executing code that normally exists in ROM in RAM, because the RAM devices operate faster than the ROM devices normally used.

RAM Footprint

The latest Power Macintosh G3 computer has its Mac OS ROM image stored in RAM. This removes approximately 3 megabytes of RAM from availability for other uses. In effect, a system with 32 megabytes of RAM appears to have only 29 megabytes available. Some portion of the missing 3 megabytes is offset by having fewer patches in RAM. Other mechanisms are being explored in an attempt to minimize the impact of ROM-in-RAM.

User Experience

Setting the boot volume from the Startup Disk control panel makes all the changes to the boot process that are necessary to operate with a Mac OS ROM image in RAM. The control panel user interface remains unchanged for this release.

Data Structures and Files

The Mac OS ROM image is contained in a new file, named “Mac OS ROM”, that is kept in the System Folder. The Mac OS ROM image is exactly the same as it would be if it were an actual Mac OS ROM, containing the high-level software, the kernel software, and the 68K emulator.

The Startup Disk control panel sets the Open Firmware’s boot-device configuration variable by modifying the Open Firmware NV-RAM partition that contains the Open Firmware’s configuration variables. The format of the NV-RAM partition is defined in the Open Firmware CHRP Binding. The partition is accessed using RTAS.

Compatibility

A Mac OS ROM image that is in write-protected RAM will appear to be a ROM to all MacOS software and applications. Because the image of the Mac OS ROM in RAM appears to be a ROM, the ROM-in-RAM approach is completely compatible with all application and system software.

The Mac OS ROM image is kept in a file in the System Folder on the specified boot device. In order to avoid problems with localizing the name, the file is located by file type instead of by name.

In order for Open Firmware to retrieve the Mac OS ROM image file, it must be able to read the selected boot device. If the Mac OS ROM image file is on a partition that is on a RAID, encrypted, striped, or otherwise non-standard device, Open Firmware must be able to read from these devices in order to boot the Mac OS. Two possible solutions to this problem are to have a standard partition available on the device that contains the Mac OS ROM image file, or to provide Open Firmware methods to read the file.

The main incompatibility that ROM-in-RAM approach introduces is that memory is not mapped one-to-one, as it has been for previous PCI-based Macs. Software that assumes the logical and physical addresses are the same will fail, even when virtual memory is not on. Well-behaved software—that is, software that calls the `LogicalToPhysical` or `PrepareMemoryForIO` functions when it needs a physical memory address—will continue to work.

IMPORTANT

Designers of DMA device drivers should refer to *Designing PCI Cards and Drivers for the Power Macintosh* for a information about using the `PrepareMemoryForIO` function to set up mapping for physical and logical addresses. The relevant section is on pages 219–229. For device drivers running with the NewWorld software, the sentence on page 227 that says “Certain DMA transactions require both mapping tables” should be interpreted to mean “All DMA transactions...”

Boot ROM Contents

The boot ROM contains the code needed to start up the computer, initialize and examine the hardware, provide a device tree to describe the hardware, provide hardware access services (RTAS), and control to the operating system. The boot ROM can be grouped into the following major pieces.

POST Code

The Power-on Self Test (POST) software is executed when the computer first boots. This encompasses many of the traditional Macintosh ROM operations and is based on the hardware initialization code used in the past: setup and initialization of the processor and ASICs, a boot beep, an error beep, diagnostics, and transfer to Open Firmware.

A small debugging mini-nub is part of this section. It allows prodding and poking with some MacsBug-like commands. Getting into the debugger nub is not possible using standard user interface input, however.

Failure to boot in POST causes the error beep, optionally entering the mini-nub.

Open Firmware

The Open Firmware component of NewWorld is based on the CHRP version of Open Firmware, also known as Open Firmware 3.0. This is the most robust and full-featured Open Firmware used by Apple to date. This version of Open Firmware contains several notable changes from the Open Firmware found in the first and second generation PCI Macintosh computers:

- Open Firmware is capable of reliably reading files from block devices.
- Open Firmware builds an expanded device tree that holds every facet of hardware information needed by an operating system.
- Open Firmware contains code that mimics the `StartSearch` code in the Mac OS ROM and provides a Mac-like user interface during startup.
- Open Firmware creates an interrupt tree that is interlaced through the device tree to provide a mechanism to describe the interrupt layout of the computer.

If a boot failure occurs in Open Firmware, Open Firmware attempts to provide a Macintosh-like experience.

Mac OS `'ndrv'` Drivers

The boot ROM may also contain Mac OS drivers that are hardware-specific and needed at boot time; they are organized as `'ndrv'` drivers. Drivers needed at boot time (video drivers, network drivers, or disk drivers) need to be loaded from the device tree.

RTAS

RTAS (Run-Time Abstraction Services) can be thought of as a BIOS (basic input/output system). RTAS code handles hardware accesses needed by an operating system, making it possible for multiple operating systems to get hardware services without having to know the specifics. RTAS handles hardware-specific services such as NV-RAM (containing parameter RAM), time services (the real-time clock), PCI configuration cycles, power management, and the code needed to restart and shutdown.

RTAS is relocateable code; its location in RAM is determined by the operating system, and it remains functional after the operating system boots.

Note
RTAS is part of the system software. It is not needed by applications, which use operating system APIs. ◆

Mac OS ROM Image File Contents

The Mac OS ROM image file (also called the bootinfo file) contains three main components, each of which is made up of smaller components: the pieces that are part of the bootinfo specification, the Trampoline code, and the Mac OS ROM Image itself.

Most changes needed for a new CPU occur in the boot ROM, not in the bootinfo file. Changes to the Mac OS ROM Image should be limited to new manager software and support for hardware that is common to many Macintosh computers (ATA interface modules, user interface modules, and the like).

The bootinfo file exists on the boot device and has a localizable name. Identification information that leads to the file's path is stored in NV-RAM and the search algorithm for a usable bootinfo file parallels the search mechanism across SCSI, ATA, and so forth, used in the former startup disk routine. By default, the file is located by using the directory ID of the "blessed folder" in the boot block of each HFS or HFS Plus partition, and then searching for a file with a file type of `'tbxi'`. Searching by file type is done to allow localization of the file. Nonlocalized, the name of the bootinfo file is "Mac OS ROM".

Open Firmware Script

The bootinfo components normally do not need to be changed for each new product. The Open Firmware script is automatically modified at build time to have the correct offsets within the bootinfo file to the other two main components.

Trampoline Code

The Trampoline code is the component of the NewWorld architecture that handles the transition between Open Firmware and the Mac OS ROM Image. It retrieves all necessary information about the system from Open Firmware, instantiates RTAS, decompresses the Mac OS ROM Image, locates the Mac OS NV-RAM partition, formats the system information into tables and data structures for the Mac OS, terminates Open Firmware, moves information in memory to safe locations, and transfers control to the Mac OS ROM Image.

Mac OS ROM Image

The NewWorld version of the Mac OS ROM Image is similar to the old Mac OS ROM in that it has a similar layout and contains many of the same components as it did before.

The Mac OS ROM Image includes code that contains hardware-specific support, including ADB, VIA, Cuda/Egret, MESH SCSI, and the Heathrow/CHRP/UltraDMA AIMs. In the future, that code can be moved out of the Mac OS ROM Image when there is a mechanism to load it from a boot volume at boot time.

NewWorld Boot Process

Here is a high-level view of the execution path take when a NewWorld-based computer boots.

1. The POST code runs (preliminary diagnostics, boot beep, initialization, and setup), with possible intervention in the mini nub, a small debugging tool.
2. Open Firmware initializes and begins execution, including building the device tree and the interrupt trees.

3. Open Firmware loads the Mac OS ROM image file, based on defaults and NV-RAM settings.
4. Open Firmware executes the Forth script in the bootinfo file, which contains instructions to read both the Trampoline code and the compressed Mac OS ROM Image and place them into a temporary place in memory.
5. The Forth script transfers control to the Trampoline code, which functions as the transition between Open Firmware and the beginning of the Mac OS execution.
6. The Trampoline code decompresses the Mac OS ROM Image, gathers information about the system from Open Firmware, creates data structures based on this information, terminates Open Firmware, and rearranges the contents of memory to an interim location in physical memory space.
7. The Trampoline code transfers control to the `HardwareInit` routine in the Mac OS ROM Image.
8. The `HardwareInit` routine copies data structures to their correct places in memory, and then calls the NanoKernel.
9. The NanoKernel fills in its data structures and then calls the 68K emulator.
10. The 68K emulator initializes itself, then transfers control to the startup initialization code.
11. The startup initialization code begins execution, initializing data structures and managers, and booting the Mac OS.

All functions found in the old Mac OS ROM are present in the NewWorld boot process, but occur at different times and places. To accomplish this, the code in the Mac OS ROM Image and POST is simplified, while the Trampoline code addresses the new functionality.

What Is Different

Even though ROM-in-RAM involves a fundamental change to the construction of the product-specific part of the Mac OS, the changes in the code and its execution are not that large. Many components are in changed locations, but their functions with respect to boot time and run time have not greatly changed. Many Mac OS components remain untouched.

Interrupt Handling

Interrupt handling is very different with the NewWorld approach. The interrupt code has been rewritten to allow for dynamic creation of the interrupt layout. The new code has two features that did not exist in the old code. One is that interrupt latency has been reduced to such an extent as to make it negligible. The other is that the interrupt handling code no longer requires changes to support a new machine unless it has new interrupt controller hardware. The description of the interrupt layout is now part of an Open Firmware interrupt tree that is interlaced within the Open Firmware device tree. The Trampoline code uses this interrupt tree to build the Mac OS native interrupt tree.

Outmoded Resources

Prior to the NewWorld architecture, many resources in the ROM existed in the System Folder as well, often as replacements that fix or enhance those in the ROM, but sometimes merely because the ROM resources have not yet been removed from the ROM. With the NewWorld approach, any resources that are not needed early in the boot sequence are no longer in the Mac OS ROM Image, and only the resources from the System Folder are in use.

RAM Footprint

The NewWorld architecture puts the Mac OS ROM Image in RAM, and marks it read-only. Although the image is 4 megabytes in size, not all of it is in use. The portion that is not used is returned to the Mac OS for use as part of system RAM. At the time this document was written, less than 3 megabytes of the 4 megabyte Mac OS ROM Image are in use, allowing more than 1 megabyte to be returned to the Mac OS.

RTAS

Certain hardware devices differ from machine to machine, but provide similar functions. RTAS (Run-time Abstraction Services) provides such hardware-specific functions, including functions for accessing the real-time clock, nonvolatile RAM (NV-RAM), restart, shutdown, and PCI configuration cycles. The I/O primitives for these functions in the Mac OS ROM Image for NewWorld use RTAS.

NV-RAM

Instead of using hard-coded offsets to locations in NV-RAM for Mac OS NV-RAM and other information, the Trampoline code breaks NV-RAM into variable-sized partitions that are used by Mac OS, Open Firmware, and any other client. PRAM resides in the Mac OS partition. The partitioning scheme is part of the CHRP specification.

NanoKernel

The previous version of the NanoKernel has code that is processor-specific to create data structures. With the NewWorld architecture, the Trampoline code creates these data structures from information in the Open Firmware device tree.

NanoKernel is typically no longer changed to support a new CPU. Support for new processors has moved to POST, which is responsible for configuring all processor-specific registers. Runtime cache control is part of RTAS.

Startup Disk Control Panel

Open Firmware now bears responsibility for locating a startup device. This is very different from previous Mac OS systems where the Mac OS ROM had responsibility for locating the startup device. On the Power Macintosh G3 computer, the Mac OS ROM image itself comes from the startup disk, so decisions regarding startup device must be made earlier in the startup process. Open Firmware recreates as much as possible the user experience of earlier systems but the implemention is very different.

Previous systems stored the user's selected startup device in PRAM. The startup device was set in PRAM when the user selected a device in the Startup Disk control panel. This device was honored by the Mac OS ROM unless the selected device was unavailable or was overridden by the user.

The startup disk routine for the latest Power Macintosh G3 computer, rather than setting Mac OS PRAM, sets an Open Firmware config variable called `boot-device`. This setting is honored by Open Firmware unless the selected device was unavailable or was overridden by the user.

The following keys can be used to override the selected startup device.

- Command-Option-Shift-Delete: ignore the boot-device setting and scan for alternate devices.

- C: force the internal CD-ROM drive to be the startup device
- D: force the internal hard disk to be the startup device

Once Open Firmware locates a startup device and successfully loads a Mac OS ROM image, it passes information about the chosen device in the bootpath variable. This information, rather than that previously set in PRAM, is subsequently used by the Mac OS ROM to locate the device containing the startup System Folder.

IMPORTANT

The previous API for controlling the startup device selection, using `_GetDefaultStartup` and `_SetDefaultStartup`, is not effective on the latest Power Macintosh G3 computer. ▲

Open Firmware and the Device Tree

NewWorld relies heavily on a functioning Open Firmware with a complete device tree. For each device that is supported by a PCI expansion card, the device-tree information is provided by startup code in the expansion ROM on the card. For a discussion of the levels of support such cards can provide, please see the section "Device Configuration" starting on page 32 of *Designing PCI Cards and Drivers for Power Macintosh Computers*.

Open Firmware and Startup Devices

In order for a device supported by a PCI expansion card to participate in the startup process, the card must include an expansion ROM containing startup firmware. Startup firmware is written in the Forth language, as defined by IEEE Standard 1275, and is stored in an abbreviated representation called FCode. The startup firmware in the Power Macintosh ROM includes an FCode loader that installs FCode in the system RAM so that drivers can run on the PowerPC main processor.

Device drivers that are required during system startup (called Open Firmware drivers) are also written in FCode. Expansion cards for startup devices must contain all the driver code required during startup in the expansion ROM on the card. Depending on their functions, such cards may also need to provide support resources such as fonts. Examples of devices needed during system

startup include display, keyboard, and mouse devices, and storage devices such as hard drives and CD-ROM drives.

IMPORTANT

If Open Firmware code is not included in the expansion card for a startup device, the card will not be usable until the operating system loads its supporting software from disk after the startup process has concluded. ▲

For a description of the way startup code in an expansion card's ROM exports properties to the Open Firmware device tree, please see *Designing PCI Cards and Drivers for Power Macintosh Computers.*

Interrupt Layout

The interrupt layout is determined by information in the device tree. An interrupt tree overlays the other information in the device tree to describe how the interrupts are configured. The Trampoline code traverses this device tree interrupt tree and builds data structures that are used to dispatch interrupts. The device tree interrupt tree is defined in the *Open Firmware Recommended Practice: Interrupt Mapping*. It is not necessary to change any of the interrupt dispatching code, either 68K or native. All the necessary information is retrieved from the device tree.

This interrupt dispatch code has drastically reduced latency times as compared to all previous PCI Macintosh computers.

Machine Identification

Because the NewWorld architecture uses the same Universal and ProductInfo tables for all computer models that it runs on, those computers all have the same Box Flag. All those computers use the same enablers, and no patches are made to the Mac OS ROM Image, so sharing the same box flag is not an issue for those areas.

IMPORTANT

Programs such as control panels and installers that use Box Flag to verify that this is a valid CPU on which to execute need to be changed to verify the existence of the hardware they require. Developers should look for the features they need, rather than reading the box flag and then making assumptions about the computer's features. ▲

Asset management software that reports the kind of machine it is run on should check the name registry for the value of the property at `Devices:device-tree:model`. For the current Power Macintosh G3 computer, the model property value is "`PowerMac1,1`".

Conventions and Abbreviations

This developer note uses the following typographical conventions and abbreviations.

Typographical Conventions

Note
A note like this contains information that is of interest but is not essential for an understanding of the text. ◆

IMPORTANT
A note like this contains important information that you should read before proceeding. ▲

Abbreviations

When unusual abbreviations appear in this developer note, the corresponding terms are also spelled out. Standard units of measure and other widely used abbreviations are not spelled out.

Here are the standard units of measure used in developer notes:

A	amperes	lb.	pounds
dB	decibels	mA	milliamperes
bps	bits per second	µA	microamperes
GB	gigabytes	MB	megabytes
Hz	hertz	Mbps	megabits per second
in.	inches	MHz	megahertz
k	1000	mm	millimeters
K	1024	ms	milliseconds
KB	kilobytes	µs	microseconds
kbps	kilobits per second	ns	nanoseconds

kg	kilograms	sec.	seconds
kHz	kilohertz	V	volts
kΩ	kilohms	W	watts

Other abbreviations used in developer notes include these:

$*n*	hexadecimal value *n*
ADB	Apple Desktop Bus
ATA	advanced technology attachment
ATAPI	advanced technology attachment with packet interface
AV	audio/visual
BIOS	basic input/output system
CAS	column address strobe
CD-ROM	compact disc read-only memory
CRM	Communications Resource Manager
DAC	digital to analog converter
DDC	display data channel
DIMM	dual inline memory module
DIN	Deutsche Industrie Norm
DMA	direct memory access
DRAM	dynamic random-access memory
DVD	digital video disc, also referred to as digital versatile disc
EDO	extended data out DRAM device type
EMI	electromagnetic interference
GCR	group code recording
HID	human interface device, a class of USB devices
IC	integrated circuit
IIC	inter-integrated circuit (an internal control bus)
I/O	input/output
IR	infrared
IrDA	Infrared Data Association
ISO	International Organization for Standardization

JEDEC	Joint Electronics Devices Engineering Council
L2	level 2, used in reference to level of cache
LVD or LVDS	low voltage differential signaling
Mac OS	Macintosh operating system
MESH	Macintosh enhanced SCSI hardware
MMU	memory management unit
MPEG	Motion Picture Experts Group
NTSC	National Television Standards Committee (the standard system used for broadcast TV in North America and Japan)
PAL	Phase Alternating Line system (the standard for broadcast TV in most of Europe, Africa, South America, and southern Asia)
PCI	Peripheral Component Interconnect
PGA	pin grid array
PIO	parallel input output
RAM	random-access memory
RAS	row address strobe
RAVE	Rendering Acceleration Virtual Engine
RGB	a video signal format with separate red, green, and blue components
RISC	reduced instruction set computing
ROM	read-only memory
SCSI	Small Computer System Interface
SCC	serial communications controller
SDRAM	synchronous dynamic random-access memory
SECAM	the standard system used for broadcast TV in France and the former Soviet countries
SGRAM	synchronous graphics random-access memory
SO-DIMM	small outline dual inline memory module
SRAM	static random-access memory
S-video	a type of video connector that keeps luminance and chrominance separate; also called a Y/C connector

USB	Universal Serial Bus
VRAM	video RAM; used for display buffers
Y/C	a type of video connector that keeps luminance and chrominance separate; also called an S-video connector
YUV	a video signal format with separate luminance and chrominance components

Index

A

abbreviations 85 to 88
ADB (Apple Desktop Bus) port 42
ADB connector 42
address multiplexing for RAM DIMMs 65
ATA-3 52
ATA / ATAPI-4. *See* Ultra DMA / 33 hard disk
ATA hard disk drive 52
ATI 3D RAGE 128 GL IC 38

B

back view of enclosure 22
block diagram of main logic board 33
boot ROM 71
  contents of 74 to 76
box flag 82
Burgundy custom IC 37

C

cache expansion 29
CD-ROM drive 52
communications slot 67
compatibility
  CD-ROM, DVD-ROM, Zip drive 29
  L2 cache 29
  modem slot 27
  power supply 29
  SCSI devices 29
connectors
  ADB 42
  FireWire 49
  internal hard disk drive 52
  monitor 56
  sound input jack 54
  sound output jacks 54
  USB 44
Cuda IC 38
custom ICs 35
  Burgundy 37
  Cuda 38
  Grackle 36
  Paddington 37

D

DDC monitors 57
device tree 77, 81
DIMMs. *See* RAM DIMMs
disk drives 51 to 53
display memory 39
displays
  adapter for 57
  DDC monitors 57
  monitor sense codes 89
  sense codes 57
DVD-ROM drive 53

E

enclosure
  back view 22
  front view 21
Ethernet port 50
expansion bus. *See* PCI expansion bus
expansion slots 28, 66

F

FCode 81
features summary 18
FireWire
  controller 40
  link layer 40
FireWire ports 48
  connectors 49
front view of enclosure 21

G

Grackle custom IC 36
graphics controller 38

H

hard disk drive 52

I

internal modem (optional) 40, 51
interrupts 79, 82
I/O control IC. *See* Paddington custom IC
I/O ports
  ADB 42
  Ethernet 50
  FireWire 48
  monitor 56
  optional internal modem 51
  sound 53
  USB 43

K

keyboard 46 to 48
  and USB 47

M

machine identification 82
Macintosh ROM, why it's changing 70 to 74
Mac OS Image file, contents of 76 to 77
  Mac OS ROM Image 77
  Open Firmware script 77
  Trampoline Code 77
Mac OS ROM 71
Mac OS ROM file 73
Mac OS ROM Image 72, 77
Mac OS software 71
memory control IC 36
microphone 54
modem interface 51
modem slot 67
monitor adapter 57
monitor sense codes 57
mouse 48

N

NanoKernel 80
'ndrv' drivers 75
NewWorld software architecture 70 to 83
  boot process 77 to 78
  boot ROM 71
  compatibility with applications 73
  data structures and files 73
  features 72 to 74
  performance 72
  RAM footprint 73, 79
  user experience with 73
  what has changed 71, 78 to 83
  with Open Firmware 71, 72
  with POST code 72
  with RTAS 72
nonvolatile RAM. *See* NVRAM
NVRAM 37, 80

O

OHCI controller for USB 46
Open Firmware, with the NewWorld architecture 71, 74, 75
Open Firmware drivers 82
Open Firmware Script 77
outmoded resources 79

P

Paddington custom IC 37
PCI bus bridge 36
PCI expansion bus 66
PCI expansion slots 66
POST code 72, 75, 77
power-on system test. *See* POST code
power supply 29

R

RAM DIMMs 64, 64 to 66
  address multiplexing for 65
  devices in 65, 66
  dimensions of 28
  installation of 64
  specifications of 64
resources, outmoded 79
ROM-in-RAM approach 74
RTAS (Run-Time Abstraction Services) 72, 76, 79
Run-Time Abstraction Services. *See* RTAS

S

screen buffers 39
SDRAM devices 66
  access time of 66
sound 54
  inputs 54
  outputs 53
  sampling rates 55
sound IC 37
sound input jack 54
sound output jacks 54
startup devices 81
Startup Disk control panel 80
startup firmware 81
summary of features 18

T

Trampoline code 77, 78

U

Ultra2 SCSI (LVD) hard disk drive 29, 52
Ultra DMA / 33 hard disk drive 51, 52
Universal Serial Bus. *See* USB entries
USB and keyboard 47
USB connectors 44
USB controller IC 39
USB ports 43 to 46
  compatibility 45 to 46
    with ADB 45
    with serial ports 45
  connectors 44
  controller type 46
  data transfer speeds 44
  transfer types 44

V

video monitors
  colors displayed 59
  DDC monitors 57
  sense codes 57
voltage switch 29

Z

Zip drive 53

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