



Developer Note

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# Macintosh LC 475 and Macintosh Quadra 605



**Developer Note**

Developer Press

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# About This Note

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This developer note provides information about the Macintosh LC 475 and Macintosh Quadra 605 computers, Apple's lowest-priced models with MC68040 microprocessors. Those computers are low-profile models with separate video monitors.

**Note**

While every attempt has been made to verify the accuracy of the information presented here, it is subject to change without notice. The primary reason for releasing this type of product information is to provide the development community with essential product specifications, theory, and application information for the purpose of stimulating work on compatible third-party products. ♦

## Contents of This Note

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The information is arranged in four chapters, an appendix, an index, and a set of foldouts:

- Chapter 1, "Introduction," gives a summary of the features and describes the external features of the Macintosh LC 475 and Macintosh Quadra 605 computers.
- Chapter 2, "Architecture," describes the internal organization of the computers. It includes a block diagram, a simplified address map, and descriptions of the integrated circuits that are specific to these computers.
- Chapter 3, "Expansion," describes the expansion slot and gives guidelines for designing an expansion card to plug into it.
- Chapter 4, "Software," summarizes the new features of the ROM software and the system software.
- The foldouts provide engineering specifications and mechanical drawings for the expansion card.

## Supplemental Reference Documents

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To supplement the information in this developer note, developers should have copies of the appropriate Apple reference books, including *Inside Macintosh*, Volumes IV, V, and VI; *Guide to the Macintosh Family Hardware*, second edition; and *Designing Cards and Drivers for the Macintosh Family*, third edition. These books are available in technical bookstores and through APDA.

## P R E F A C E

The Macintosh LC 475 and Macintosh Quadra 605 computers are similar to certain earlier Macintosh models, so you should also have the developer note that describes those earlier machines:

■ *Macintosh Developer Note Number 3*, APDA catalog number R0461LL/A

Developer notes are available from APDA and are also on the developer CDs; Number 3 has been available since March 1993.

### Note

*Macintosh Developer Note Number 3* covers the Macintosh Color Classic®, the Macintosh LC III, the Macintosh PowerBook 165c, the Macintosh Centris 610 and 650, and the Macintosh Quadra 800. ♦

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## Conventions and Abbreviations

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This developer note uses the following typographical conventions and abbreviations.

### Typographical Conventions

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New terms appear in **boldface** where they are first defined.

Computer-language text—any text that is literally the same as it appears in computer input or output—appears in *Courier* font.

Hexadecimal numbers are preceded by a dollar sign (\$). For example, the hexadecimal equivalent of decimal 16 is written as \$10.

### Special Elements

---

This developer note has three kinds of special paragraphs—Note, Important, and Warning—and a sidebar, as shown on this page.

#### **Note**

A note like this contains information that is interesting but not essential for an understanding of the text. ◆

#### **IMPORTANT**

A note like this contains important information that you should read before proceeding. ▲

#### ▲ **WARNING**

A note like this directs your attention to something that could cause damage or result in a loss of data. ▲

## Standard Abbreviations

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When unusual abbreviations appear in this book, the corresponding terms are also spelled out. Standard units of measure and other widely used abbreviations are not spelled out. Here are the standard units of measure used this developer note:

|            |           |          |              |
|------------|-----------|----------|--------------|
| A          | amperes   | mA       | milliamperes |
| dB         | decibels  | $\mu$ A  | microamperes |
| GB         | gigabytes | MB       | megabytes    |
| Hz         | hertz     | MHz      | megahertz    |
| in.        | inches    | mm       | millimeters  |
| k          | 1000      | ms       | milliseconds |
| K          | 1024      | $\mu$ s  | microseconds |
| KB         | kilobytes | ns       | nanoseconds  |
| kg         | kilograms | sec.     | seconds      |
| kHz        | kilohertz | V        | volts        |
| k $\Omega$ | kilohms   | W        | watts        |
| lb.        | pounds    | $\Omega$ | ohms         |

Here are other abbreviations used in this developer note:

|        |   |
|--------|---|
| $\$n$  | hexadecimal value <i>n</i>                                  |
| AC     | alternating current   |
| ADB    | Apple Desktop Bus   |
| CD-ROM | compact-disk read-only memory                               |
| CLUT   | color lookup table  |
| EMI    | electromagnetic interference                                |
| FPU    | floating-point unit   |
| IC     | integrated circuit  |
| I/O    | input/output  |
| LS     | low-power Schottky (used as a standard for IC device loads) |
| MMU    | memory management unit                                      |
| MOS    | metal-oxide semiconductor                                   |
| NMI    | nonmaskable interrupt                                       |
| PWM    | pulse-width modulation                                      |
| RAM    | random-access memory  |
| RMS    | root-mean-square  |
| ROM    | read-only memory  |
| SANE   | Standard Apple Numerics Environment                         |
| SCSI   | Small Computer System Interface                             |

## P R E F A C E

|      |   |
|------|---|
| SCC  | serial communications controller  |
| SIMM | single inline memory module   |
| SWIM | Super Woz Integrated Machine, a custom IC that controls the floppy disk interface |
| TTL  | transistor-transistor logic (used as a standard for IC device loads)              |
| VLSI | very large scale integration  |
| VRAM | video RAM   |



# Introduction

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## Introduction

The Macintosh LC 475 and Macintosh Quadra 605 computers bring the high performance of the MC68040 microprocessor to low-priced Macintosh models. These computers are low-profile designs, mechanically similar to the Macintosh LC III.

## Summary of Features

---

Here is a summary of the hardware features of the Macintosh LC 475 and Macintosh Quadra 605 computers:

- Motorola MC68LC040 microprocessor (no FPU) running at 25 MHz
- installed RAM capacity of 4 MB, expandable to 36 MB
- 1 MB ROM soldered to main logic board
- low-profile design with external video monitor
- built-in video hardware using separate video RAM
- internal hard disk with 80 MB or 160 MB capacity (or 230 MB on Macintosh LC 475 ), using the internal SCSI connector; external SCSI port for additional SCSI devices
- internal high-density floppy disk drive with 1.4 MB capacity
- standard Macintosh I/O ports: two serial ports, sound output jacks, a SCSI port, and an ADB port
- sound input jack
- internal speaker
- expansion slot for 96-pin or 114-pin expansion cards (accepts PDS cards designed for the Macintosh LC series; not directly connected to the MC68LC040 processor)

Electrically, the Macintosh LC 475 and Macintosh Quadra 605 computers are similar to the Macintosh Centris 650. Table 1-1 compares the features of those computers.

**Table 1-1** Comparisons with the Macintosh Centris 650 computer

| <b>Features</b>    | <b>Macintosh Centris 650</b>                     | <b>Macintosh LC 475 and Macintosh Quadra 605</b>   |
|--------------------|--|--|
| Processor type     | MC68LC040  | MC68LC040  |
| Processor speed    | 25 MHz   | 25 MHz   |
| Amount of RAM      | 4 MB–136 MB                                      | 4 MB–36 MB   |
| RAM expansion      | 4 SIMMs  | 1 SIMM   |
| Amount of VRAM     | 512 KB–1 MB                                      | 512 KB–1 MB  |
| Sound capabilities | 8 bits/channel; mono in, mono record, stereo out | 8 bits/channel; stereo in, mono record, stereo out |

*continued*

**Table 1-1** Comparisons with the Macintosh Centris 650 computer (continued)

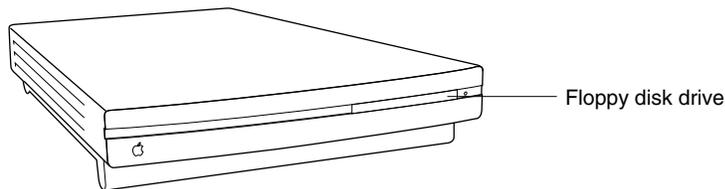
| Features             | Macintosh Centris 650    | Macintosh LC 475 and Macintosh Quadra 605                     |
|----------------------|--------------------------|---|
| Floppy disk drive    | 1 internal               | 1 internal  |
| ADB ports            | 2                        | 1   |
| Internal SCSI drives | 2 (hard disk, CD-ROM)    | 1 (hard disk)   |
| External SCSI ports  | 1                        | 1   |
| Ethernet             | optional, internal       | no  |
| Expansion slots      | 1 PDS,<br>3 NuBus™ slots | 1 I/O slot<br>(compatible with Macintosh LC series PDS cards) |

## Appearance

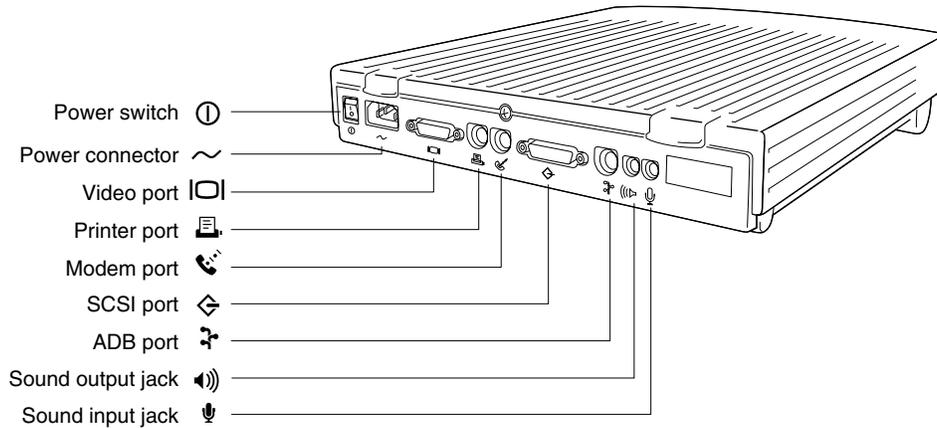
The Macintosh LC 475 and Macintosh Quadra 605 computers have similar low-profile designs.

### Views of the Macintosh LC 475 Computer

The design of the Macintosh LC 475 computer is similar to that of the Macintosh LC III. Figure 1-2 shows the front of the Macintosh LC 475 computer. Figure 1-2 shows the back of the Macintosh LC 475 computer and identifies the I/O ports.

**Figure 1-1** Front view of the Macintosh LC 475 computer

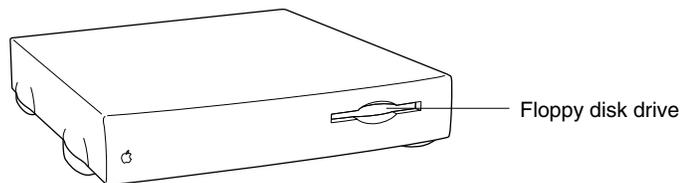
**Figure 1-2** Back view of the Macintosh LC 475 computer



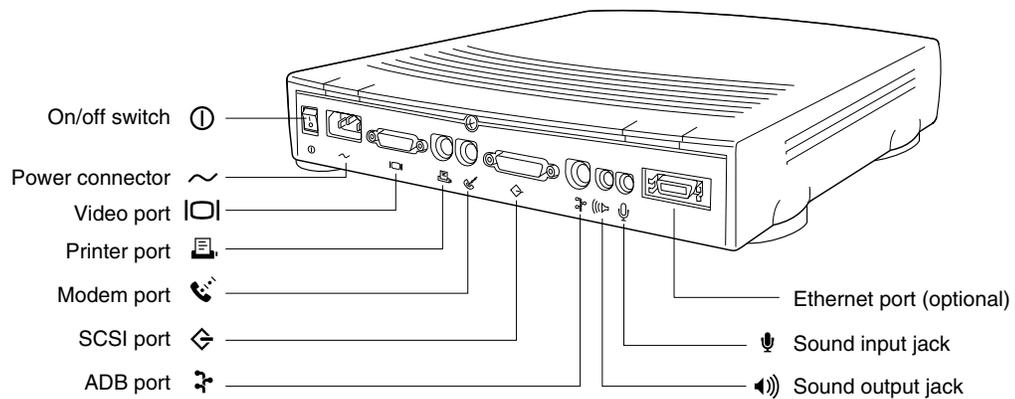
## Views of the Macintosh Quadra 605 Computer

The Macintosh Quadra 605 computer is about the same size as the Macintosh LC 475. Figure 1-3 shows the front of the Macintosh Quadra 605 computer. Figure 1-4 shows the back of the Macintosh Quadra 605 computer and identifies the I/O ports.

**Figure 1-3** Front view of the Macintosh Quadra 605 computer



**Figure 1-4** Back view of the Macintosh Quadra 605 computer



## External Video Monitors

---

The Macintosh LC 475 and Macintosh Quadra 605 computers require an external video monitor. These computers can work with several sizes of video monitors.

Table 1-2 shows the maximum pixel depths available for different monitor screen sizes and amounts of VRAM. The maximum pixel depth available depends on the size of the monitor's screen and on the amount of VRAM installed. For information about VRAM expansion, see "Video RAM" on page 13.

For more information about the video monitors, see "Video Timing Parameters" on page 28.

**Table 1-2** Maximum pixel depths for the two VRAM sizes

| Monitor type       | Monitor screen size in pixels | Maximum pixel depth with 512 KB VRAM | Maximum pixel depth with 1 MB VRAM |
|--------------------|-------------------------------|--------------------------------------|------------------------------------|
| 12-inch color      | 512 × 384                     | 16                                   | 16                                 |
| 12-inch monochrome | 640 × 480                     | 8                                    | 8                                  |
| 14-inch color      | 640 × 480                     | 8                                    | 16                                 |
| 15-inch portrait   | 640 × 870                     | 4                                    | 8                                  |
| 16-inch color      | 832 × 624                     | 8                                    | 16                                 |
| 19-inch color      | 1024 × 768                    | 4                                    | 8                                  |
| 21-inch monochrome | 1152 × 870                    | 4                                    | 8                                  |
| 21-inch color      | 1152 × 870                    | 4                                    | 8                                  |
| NTSC or VGA        | 640 × 480                     | 8                                    | 16                                 |

**Note**

By using the Monitors control panel computer, the user can select a 16-color, 560-by-384-pixel display mode when the Apple IIe Card for the Macintosh LC is installed in the expansion slot. ♦

## Video Connector

The monitor connects to the computer's DB-15 external video connector; Table 1-3 shows the pin assignments.

**Table 1-3** Pin assignments on the external video connector

| Pin   | Signal name | Description                       |
|-------|-------------|-----------------------------------|
| 1     | RED.GND     | Red video ground                  |
| 2     | RED.VID     | Red video signal                  |
| 3     | /CSYNC      | Composite synchronization signal  |
| 4     | SENSE0      | Monitor sense signal 0            |
| 5     | GRN.VID     | Green video signal                |
| 6     | GRN.GND     | Green video ground                |
| 7     | SENSE1      | Monitor sense signal 1            |
| 8     | n.c.        | Not connected                     |
| 9     | BLU.VID     | Blue video signal                 |
| 10    | SENSE2      | Monitor sense signal 2            |
| 11    | GND         | CSYNC and VSYNC ground            |
| 12    | /VSYNC      | Vertical synchronization signal   |
| 13    | BLU.GND     | Blue video ground                 |
| 14    | HSYNC.GND   | HSYNC ground                      |
| 15    | /HSYNC      | Horizontal synchronization signal |
| Shell | SGND        | Shield ground                     |

### Note

The video connector on the Macintosh LC 475 and Macintosh Quadra 605 computers is the same as the one on the Macintosh LC III. ♦

## Monitor Sense Codes

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To identify the type of monitor connected, the computers use the Apple monitor sense codes and the extended sense codes. Table 1-4 shows the sense codes for each of the monitors that the Macintosh LC 475 and Macintosh Quadra 605 computers support. Refer to the Macintosh Technical Note *M.HW.SenseLines* for a description of the sense code system.

**Table 1-4** Monitor sense codes

| Monitor type     | Standard sense code | Extended sense code |       |       |
|------------------|---------------------|---------------------|-------|-------|
|                  | (SENSE2-0)          | (1,2)               | (0,2) | (0,1) |
| 12-inch RGB      | 0 1 0               | —                   | —     | —     |
| 14-inch RGB      | 1 1 0               | —                   | —     | —     |
| 15-inch Portrait | 0 0 1               | —                   | —     | —     |
| VGA              | 1 1 1               | 1 1                 | 1 0   | 1 0   |
| 16-inch RGB      | 1 1 1               | 1 0                 | 1 1   | 0 1   |
| 19-inch RGB      | 1 1 1               | 0 1                 | 0 1   | 1 1   |
| 21-inch RGB      | 0 0 0               | —                   | —     | —     |
| No monitor       | 1 1 1               | 1 1                 | 1 1   | 1 1   |

## RAM Expansion

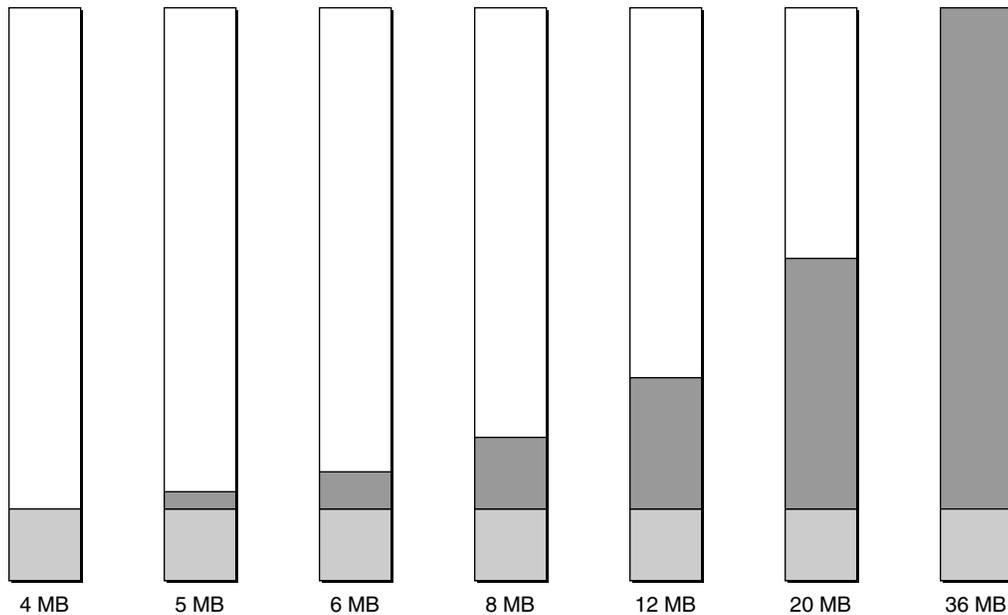
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The Macintosh LC 475 and Macintosh Quadra 605 computers come with 4 MB of RAM and 512 KB of VRAM installed. The user can expand the RAM up to a maximum of 36 MB and the VRAM to 1 MB.

### RAM Configurations

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Figure 1-5 shows the RAM configurations for different amounts of RAM. For more information, see the section “RAM Addresses” on page 26.

**Figure 1-5** RAM configurations

## RAM SIMMs

The Macintosh LC 475 and Macintosh Quadra 605 computers have one RAM expansion socket for a 72-pin RAM SIMM. The access time of the RAM devices must be 80 ns or less.

A SIMM can be either single sided or double sided. Single-sided SIMMs using 1 Mbit, 4 Mbit, or 16 Mbit devices provide RAM expansion of 1 MB, 4 MB, or 16 MB, respectively. Double-sided SIMMs using the same devices provide 2 MB, 8 MB, or 32 MB.

## RAM SIMM Signal Assignments

Table 1-5 gives the signal assignments for the pins of the RAM SIMM.

### IMPORTANT

RAM SIMMs used in Macintosh computers must meet the timing and electrical standards of those machines. SIMMs designed for other computers may not work. ▲

**Table 1-5** Signal assignments on the RAM SIMM socket

| Pin | Signal name | Description                   |
|-----|-------------|-------------------------------|
| 1   | GND         | Ground                        |
| 2   | DQ0         | Data input/output bus, bit 0  |
| 3   | DQ16        | Data input/output bus, bit 16 |
| 4   | DQ1         | Data input/output bus, bit 1  |
| 5   | DQ17        | Data input/output bus, bit 17 |
| 6   | DQ2         | Data input/output bus, bit 2  |
| 7   | DQ18        | Data input/output bus, bit 18 |
| 8   | DQ3         | Data input/output bus, bit 3  |
| 9   | DQ19        | Data input/output bus, bit 19 |
| 10  | +5V         | +5 volts                      |
| 11  | n.c.        | Not connected                 |
| 12  | A0          | Address bus, bit 0            |
| 13  | A1          | Address bus, bit 1            |
| 14  | A2          | Address bus, bit 2            |
| 15  | A3          | Address bus, bit 3            |
| 16  | A4          | Address bus, bit 4            |
| 17  | A5          | Address bus, bit 5            |
| 18  | A6          | Address bus, bit 6            |
| 19  | A10         | Address bus, bit 10           |
| 20  | DQ4         | Data input/output bus, bit 4  |
| 21  | DQ20        | Data input/output bus, bit 20 |
| 22  | DQ5         | Data input/output bus, bit 5  |
| 23  | DQ21        | Data input/output bus, bit 21 |
| 24  | DQ6         | Data input/output bus, bit 6  |
| 25  | DQ22        | Data input/output bus, bit 22 |
| 26  | DQ7         | Data input/output bus, bit 7  |

*continued*

**Table 1-5** Signal assignments on the RAM SIMM socket (continued)

| Pin | Signal name | Description                   |
|-----|-------------|-------------------------------|
| 27  | DQ23        | Data input/output bus, bit 23 |
| 28  | A7          | Address bus, bit 7            |
| 29  | A11         | Address bus, bit 11           |
| 30  | +5V         | +5 volts                      |
| 31  | A8          | Address bus, bit 8            |
| 32  | A9          | Address bus, bit 9            |
| 33  | /RAS3       | Row Address Strobe 3          |
| 34  | /RAS2       | Row Address Strobe 2          |
| 35  | —           | Reserved                      |
| 36  | —           | Reserved                      |
| 37  | —           | Reserved                      |
| 38  | —           | Reserved                      |
| 39  | GND         | Ground                        |
| 40  | /CAS0       | Column Address Strobe 0       |
| 41  | /CAS2       | Column Address Strobe 2       |
| 42  | /CAS3       | Column Address Strobe 3       |
| 43  | /CAS1       | Column Address Strobe 1       |
| 44  | /RAS0       | Row Address Strobe 0          |
| 45  | /RAS1       | Row Address Strobe 1          |
| 46  | n.c.        | Not connected                 |
| 47  | /W          | Write enable                  |
| 48  | n.c.        | Not connected                 |
| 49  | DQ8         | Data input/output bus, bit 8  |
| 50  | DQ24        | Data input/output bus, bit 24 |
| 51  | DQ9         | Data input/output bus, bit 9  |
| 52  | DQ25        | Data input/output bus, bit 25 |
| 53  | DQ10        | Data input/output bus, bit 10 |

*continued*

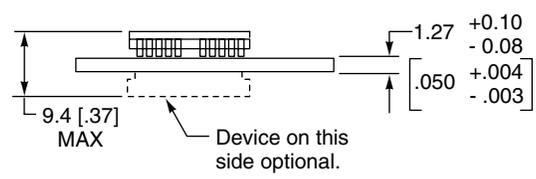
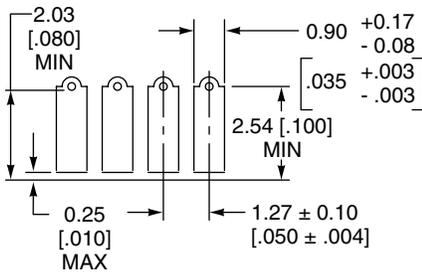
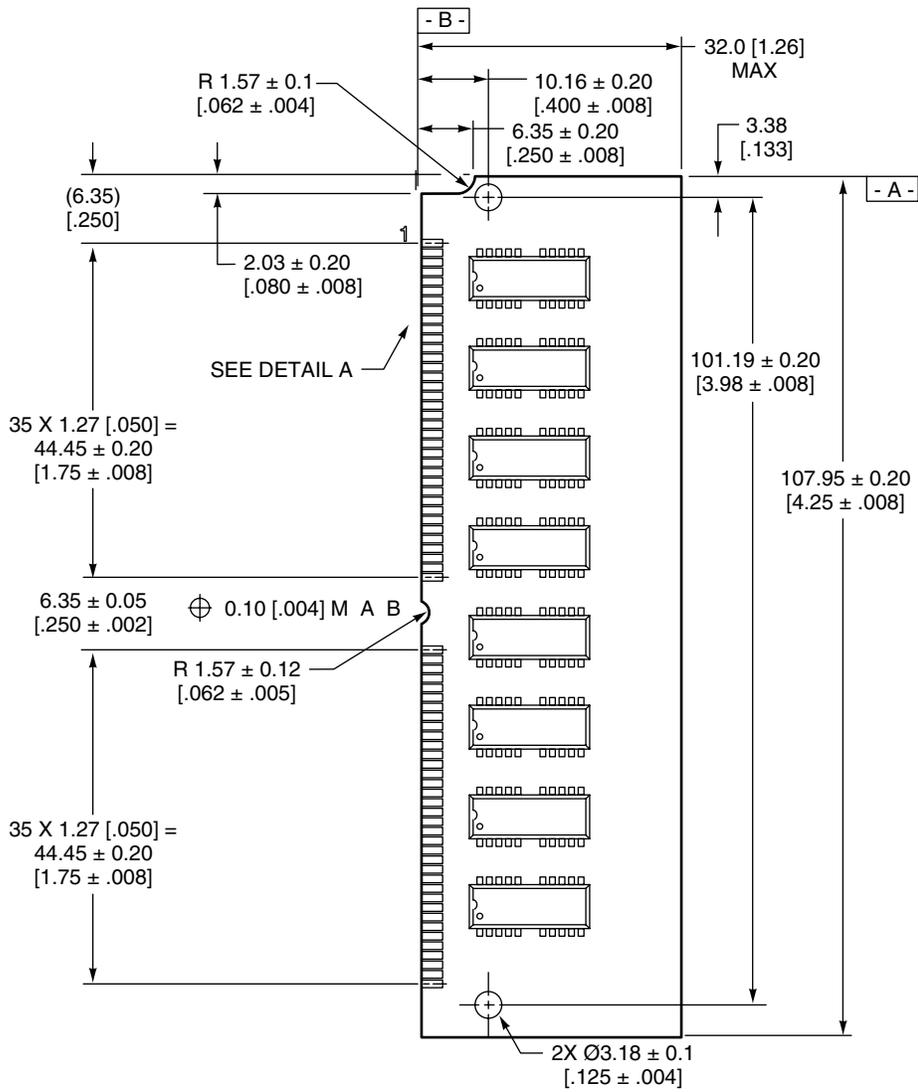
**Table 1-5** Signal assignments on the RAM SIMM socket (continued)

| Pin | Signal name | Description                   |
|-----|-------------|-------------------------------|
| 54  | DQ26        | Data input/output bus, bit 26 |
| 55  | DQ11        | Data input/output bus, bit 11 |
| 56  | DQ27        | Data input/output bus, bit 27 |
| 57  | DQ12        | Data input/output bus, bit 12 |
| 58  | DQ28        | Data input/output bus, bit 28 |
| 59  | +5V         | +5 volts                      |
| 60  | DQ29        | Data input/output bus, bit 29 |
| 61  | DQ13        | Data input/output bus, bit 13 |
| 62  | DQ30        | Data input/output bus, bit 30 |
| 63  | DQ14        | Data input/output bus, bit 14 |
| 64  | DQ31        | Data input/output bus, bit 31 |
| 65  | DQ15        | Data input/output bus, bit 15 |
| 66  | n.c.        | Not connected                 |
| 67  | —           | Reserved                      |
| 68  | —           | Reserved                      |
| 69  | —           | Reserved                      |
| 70  | —           | Reserved                      |
| 71  | n.c.        | Not connected                 |
| 72  | GND         | Ground                        |

### RAM SIMM Mechanical Specifications

The RAM SIMMs for the Macintosh LC 475 and Macintosh Quadra 605 computers are mechanically the same as the 72-pin RAM SIMMs used in the Macintosh LC III and Macintosh Centris 610 computers. The mechanical design of the RAM SIMMs is based on the industry standard design defined in the JEDEC Standard Number 21-C. Figure 1-6 shows the mechanical specifications. Pin contacts must be tin, not gold or copper, and the circuit board must dedicate one layer to power and one to ground.

Figure 1-6 RAM expansion SIMM



DETAIL A  
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## Video RAM

The video RAM works the same way on both computers. Each computer has two sockets for 68-pin VRAM SIMMs. The pair of SIMMs can contain a total of either 512 KB or 1 MB of VRAM. All the VRAM in each computer is in the SIMMs; the computers have no VRAM soldered to the logic board. The VRAM SIMMs are the same type as those used in the Macintosh LC and Centris models.

### IMPORTANT

Both VRAM SIMM sockets must be occupied and both SIMMs must be the same size, either 256 KB or 512 KB each. ▲

### Note

The system will not recognize more than 1 MB of VRAM. ◆

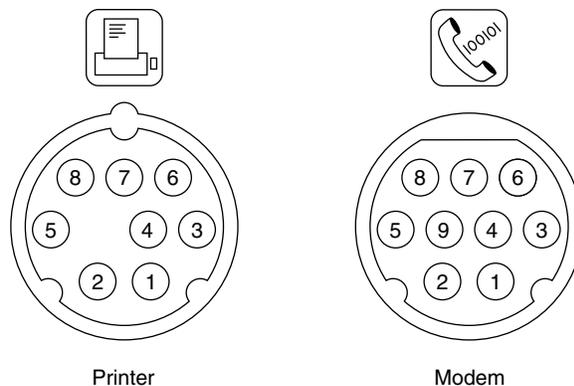
### Note

When the Apple IIe Card for Macintosh LC is installed in the expansion slot, the computer provides a 560-by-384-pixel, 16-color display for running Apple IIe software. The user selects that display mode from the Monitors control panel. For more information, see “Video Timing Parameters” on page 28. ◆

## Serial I/O Ports

The Macintosh LC 475 and Macintosh Quadra 605 computers have two serial ports, one for a printer and one for a modem. The printer port uses the standard 8-pin mini-DIN socket. The modem port uses a 9-pin mini-DIN socket. Both sockets accept 8-pin plugs, but only the modem port accepts a 9-pin plug. Figure 1-7 shows the mechanical arrangement of the pins on the serial port sockets; Table 1-6 shows the signal assignments.

**Figure 1-7** Serial port sockets



**Table 1-6** Serial port signals

| Pin number | Signal description         |
|------------|----------------------------|
| 1          | Handshake output           |
| 2          | Handshake input            |
| 3          | Transmit data -            |
| 4          | Ground                     |
| 5          | Receive data -             |
| 6          | Transmit data +            |
| 7          | General-purpose input      |
| 8          | Receive data +             |
| 9          | +5 volts (modem port only) |

Pin 9 on the modem connector provides +5V power from the ADB power supply. A modem should draw no more than 100 mA from that pin. The total current available for all devices connected to the +5V supply for the ADB and the modem port is 500 mA.

Both serial ports include the GPi (general-purpose input) signal on pin 7. The GPi signal for each port connects to the corresponding data carrier detect input on the SCC (Serial Communications Controller). On serial port A (the modem port), the GPi line can be connected to the receive/transmit clock (RTxCA) signal on the SCC. That connection supports devices that provide separate transmit and receive data clocks, such as synchronous modems. For more information about the serial ports, see *Guide to the Macintosh Family Hardware*, second edition.

## Floppy Disk Drive

The Macintosh LC 475 and Macintosh Quadra 605 computers have one internal high-density floppy disk drive (Apple SuperDrive). The drive is connected to the logic board by a 20-pin connector. Table 1-7 shows the pin assignments for the floppy disk connector.

**Table 1-7** Pin assignments for the internal floppy disk connector

| Pin number | Signal name | Signal description             |
|------------|-------------|--------------------------------|
| 1          | GND         | Ground                         |
| 2          | PH0         | Phase 0: state control line    |
| 3          | GND         | Ground                         |
| 4          | PH1         | Phase 1: state control line    |
| 5          | GND         | Ground                         |
| 6          | PH2         | Phase 2: state control line    |
| 7          | GND         | Ground                         |
| 8          | PH3         | Phase 3: register write strobe |
| 9          | n.c.        | Not connected                  |
| 10         | /WRREQ      | Write data request             |
| 11         | +5V         | +5 volts                       |
| 12         | SEL         | Head select                    |
| 13         | +12V        | +12 volts                      |
| 14         | /ENBL       | Drive enable                   |
| 15         | +12V        | +12 volts                      |
| 16         | RD          | Read data                      |
| 17         | +12V        | +12 volts                      |
| 18         | WR          | Write data                     |
| 19         | +12V        | +12 volts                      |
| 20         | n.c.        | Not connected                  |

## SCSI Bus

The Macintosh LC 475 and Macintosh Quadra 605 computers have a SCSI bus for the internal hard drive and one or more external SCSI devices.

The internal SCSI connector is a 50-pin connector with the standard SCSI pin assignments. The external SCSI connector is a 25-pin D-type connector with the same pin assignments as other Apple SCSI devices. Table 1-8 shows the pin assignments on the internal and external SCSI connectors.

**Table 1-8** Pin assignments for the internal and external SCSI connectors

| Internal (50-pin)   | External (25-pin)           | Signal name |
|---|-----------------------------|-------------|
| 2   | 8                           | /DB0        |
| 4   | 21                          | /DB1        |
| 6   | 22                          | /DB2        |
| 8   | 10                          | /DB3        |
| 10  | 23                          | /DB4        |
| 12  | 11                          | /DB5        |
| 14  | 12                          | /DB6        |
| 16  | 13                          | /DB7        |
| 18  | 20                          | /DBP        |
| 25  | –                           | n. c.       |
| 26  | 25                          | TPWR        |
| 32  | 17                          | /ATN        |
| 36  | 6                           | /BSY        |
| 38  | 5                           | /ACK        |
| 40  | 4                           | /RST        |
| 42  | 2                           | /MSG        |
| 44  | 19                          | /SEL        |
| 46  | 15                          | /C/D        |
| 48  | 1                           | /REQ        |
| 50  | 3                           | /I/O        |
| 20, 22, 24, 28,<br>30, 34, and<br>all odd pins<br>except pin 25 | 7, 9, 14, 16, 18,<br>and 24 | GND         |

## ADB Ports

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The Apple Desktop Bus (ADB) port on the Macintosh LC 475 and Macintosh Quadra 605 is functionally the same as on other Macintosh computers.

The ADB is a single-master, multiple-slave serial communications bus that uses an asynchronous protocol and connects keyboards, graphics tablets, mouse devices, and other devices to the computer. The custom ADB microcontroller drives the bus and reads status from the selected external device. A 4-pin mini-DIN connector connects the

## Introduction

ADB controller to the outside world. Table 1-9 lists the ADB connector pin assignments. For more information about the ADB, see *Guide to the Macintosh Family Hardware*, second edition.

**Table 1-9** ADB connector pin assignments

| Pin number | Name | Description  |
|------------|------|--|
| 1          | ADB  | Bidirectional data bus used for input and output. It is an open-collector signal pulled up to +5 volts through a 470-ohm resistor on the main logic board. |
| 2          | PSW  | Power-on signal that generates reset and interrupt key combinations.   |
| 3          | +5V  | +5 volts from the computer.  |
| 4          | GND  | Ground from the computer.  |

**Note**

The total current available for all devices connected to the +5V pins on the ADB and the modem port is 500 mA. Each device should use no more than 100 mA. ♦

## Sound

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Like other Macintosh computers, the Macintosh LC 475 and Macintosh Quadra 605 computers can create sounds digitally and play the sounds through their internal speakers or send the sound signals out through the sound out connector.

### Sound Input Jack

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The Macintosh LC 475 and Macintosh Quadra 605 computers have a sound input jack on the back for connecting an external microphone or other sound source. The sound input jack accepts a standard 1/8-inch phone plug, either monophonic or stereophonic (two signals plus ground).

The sound input jack accepts either the Apple PlainTalk line-level microphone or a pair of line-level signals by way of a separate adapter. The internal circuitry mixes the stereophonic signals into a monophonic signal.

**Note**

The Apple PlainTalk microphone requires power from the main computer, which it obtains by way of an extra-long, 4-conductor plug that makes contact with a 5-volt pin inside the sound input jack. ♦

**IMPORTANT**

The microphone for the Macintosh LC and LC II does not work with the Macintosh LC 475 and Macintosh Quadra 605 computers; they require the line-level signal provided by the Apple PlainTalk microphone. ▲

## Sound Modes

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The sound mode is selected by means of a call to the Sound Manager. The sound circuitry normally operates in one of four modes:

- Sound playback: computer-generated sound is sent to the speaker and the sound output jack.
- Sound playback with playthrough: computer sound and sound input are mixed and sent to the output.
- Sound record: sound input is recorded; this is the preferred method for recording, especially when using the built-in microphone.
- Sound record with playthrough: input sound is recorded and also fed through to the output.

## Sample Rates

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The Macintosh LC 475 and Macintosh Quadra 605 computers can record and play back sound at either of two sample rates: 11k samples per second and 22k samples per second. The sound circuits include input and output filters with switchable cutoff frequencies that correspond to the two sampling rates: 3.5 kHz cutoff for the 11k sample rate and 7 kHz cutoff for the 22k sample rate.

## Keyboard

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A keyboard is not included with the Macintosh LC 475 or Macintosh Quadra 605 computers, but is purchased separately.

Although the keyboard has a Power On key, identified by the symbol ⏻, the user turns the power on and off by pressing the Power switch on the back of the computer. When the user chooses Shut down from the Special menu, a dialog appears telling the user that it is now safe to shut off the computer. The user then turns off the power by pressing the power switch.

There are no programmer's switches on the Macintosh LC 475 or the Macintosh Quadra 605 computer, so the user invokes the reset and NMI functions by pressing Command key combinations while holding down the Power On key, as shown in Table 1-10. The Command key is identified by the symbols ⌘ and ⌘.

## Introduction

**Note**

The user must hold down a key combination for at least 1 second to allow the ADB microcontroller enough time to respond to the NMI or hard-reset signal. ♦

**Table 1-10** Reset and NMI key combinations

| Key combination                        | Function            |
|--|---------------------|
| Command-Power On(⌘-⌘)                  | NMI (always active) |
| Control-Command-Power On (Control-⌘-⌘) | Reset               |

**Note**

The NMI in the Macintosh LC 475 and Macintosh Quadra 605 computers can always be activated from the keyboard. This is a change from the Macintosh LC computer, where the keyboard NMI function can be deactivated by the software. ♦

## Expansion Slot

The Macintosh LC 475 and Macintosh Quadra 605 computers have a single internal expansion connector. The connector can accept either a 96-pin expansion card designed for the Macintosh LC II or a 114-pin expansion card designed for the Macintosh LC III. Chapter 3, “Expansion,” describes the signals on the expansion connector and gives guidelines for designing an expansion card for the Macintosh LC 475 and Macintosh Quadra 605 computers.

**IMPORTANT**

The expansion slot is not a PDS (processor-direct slot) because it does not connect directly to the computer’s MC68LC040 microprocessor. The expansion slot supports cards designed to work with the MC68030 microprocessor; see Chapter 3, “Expansion,” for details. ▲



# Architecture

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## Architecture

This chapter describes the architecture of the Macintosh LC 475 and Macintosh Quadra 605 computers. It describes the main components on the logic board and explains the features that are different from those of earlier Macintosh computers.

## Block Diagram and ICs

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The architecture of the Macintosh LC 475 and Macintosh Quadra 605 computers is based on the architecture of the Macintosh Centris 650. Both new computers use the MC68LC040 microprocessor and the same custom ICs, as shown in the block diagram in Figure 2-1.

The computer architecture has two internal buses. The system bus is connected directly to the MC68LC040 and runs at the same clock rate. The I/O bus is partially buffered from the MC68LC040 and runs at 16 MHz. The PrimeTime custom IC, described later, buffers the data portion of the I/O bus and provides a compatible interface for I/O devices and software designed for use with the MC68030.

### Microprocessor

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The Macintosh LC 475 and Macintosh Quadra 605 computers use the Motorola MC68LC040 microprocessor with a 25-MHz system clock. The MC68LC040 microprocessor is a low-cost version of the MC68040 without the built-in FPU. The MC68LC040 has all the other features of the MC68040; the performance of the MC68LC040 is the same as that of the MC68040 except for floating-point operations.

#### Note

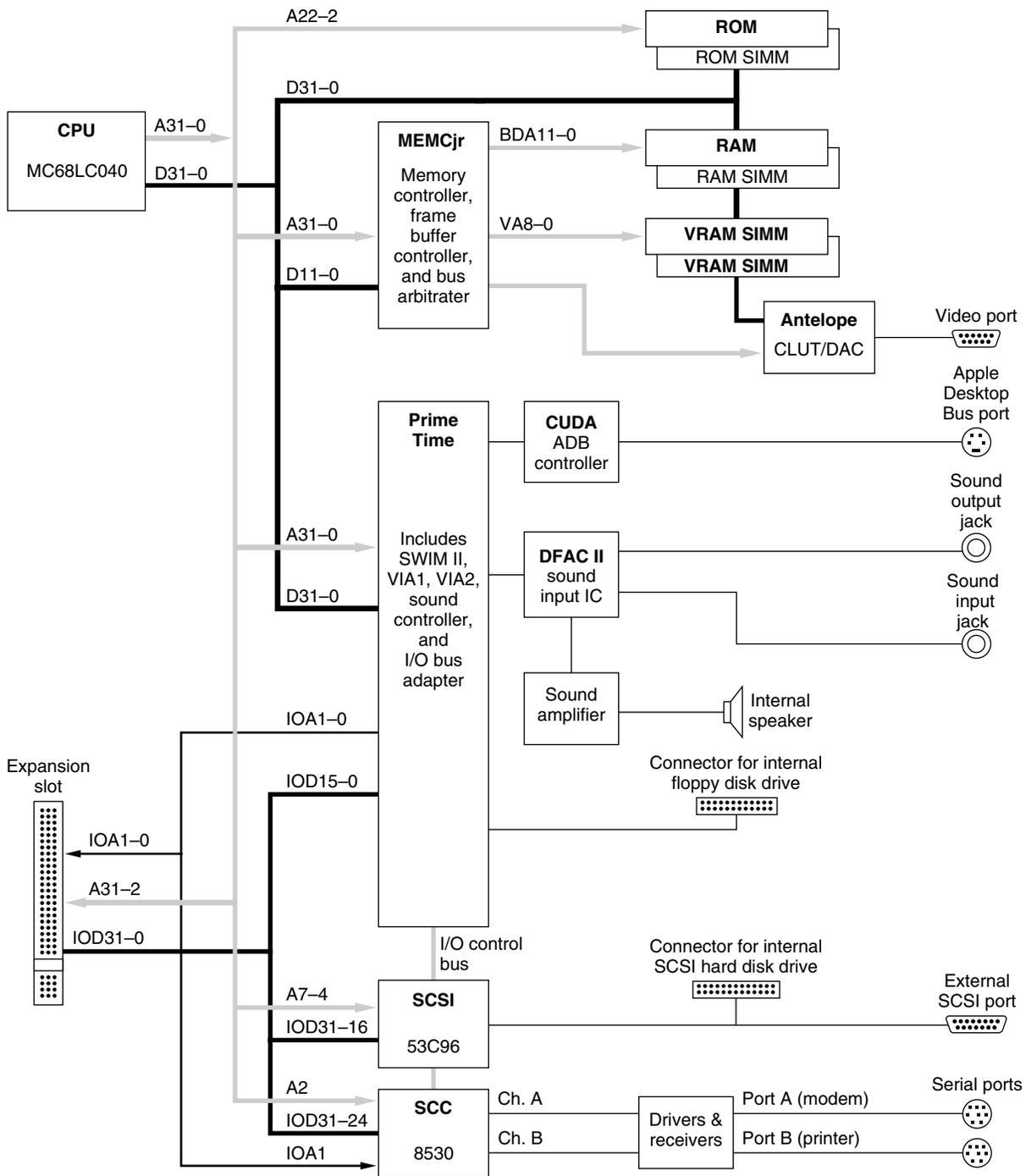
The MC68LC040 is different in many ways from the MC68020 and MC68030. For example, the built-in MMU in the MC68LC040 is not the same as the MC68851 MMU or the built-in MMU in the MC68030. Also, the caches in the MC68LC040 use a new mode called CopyBack mode. For information about these differences and the way they are reflected in the new ROM software developed for the MC68040, see Chapter 4, “Software.” For more information about cache operation in Macintosh computers, see the Technical Note *Cache as Cache Can*. ♦

In the Macintosh LC 475 and Macintosh Quadra 605 computers, the MC68LC040 microprocessor is installed in a socket. That makes it possible to upgrade to an MC68040 by removing the MC68LC040 from its socket and replacing it with the MC68040.

#### IMPORTANT

An expansion board can not provide an FPU coprocessor because the MC68LC040 microprocessor does not support the coprocessor interface and the signals on the expansion connector are not connected directly to the CPU. ▲

Figure 2-1 Block diagram



## Custom ICs

---

The Macintosh LC 475 and Macintosh Quadra 605 computers use five custom VLSI integrated circuits:

- the MEMCjr memory controller
- the PrimeTime I/O subsystem and buffer
- the DFAC II sound input processor
- the Cuda ADB controller
- the Antelope video CLUT and DAC

These computers also use several standard ICs that are used in other Macintosh computers, including the 8530 SCC serial I/O controller, and the 53C96 SCSI controller. This section describes only the custom ICs.

### MEMCjr IC

---

The MEMCjr IC combines functions performed by several ICs in previous Macintosh designs. The MEMCjr includes

- control and timing signals for the ROM, RAM, and VRAM
- control logic for system bus arbitration
- frame buffer controller for the video display

The MEMCjr IC is similar to the MEMC IC used in the Macintosh Centris 610 and 650.

#### Note

The frame buffer controller in the MEMC and MEMCjr ICs is compatible with the DAFB IC used in the Macintosh Quadra 700, 900, and 950 computers. ♦

### PrimeTime IC

---

The PrimeTime IC combines functions performed by several ICs in previous Macintosh designs. The PrimeTime IC includes

- data bus buffers for the internal I/O bus
- a SWIM II floppy disk controller
- interface adapters VIA1 and VIA2
- address decoding for I/O devices
- sound control logic and buffers

The PrimeTime IC provides the data bus features of the MC68030 that the MC68040 does not provide. Those features are **byte steering**, which allows 8-bit and 16-bit devices to be connected to a fixed byte lane, and **dynamic bus sizing**, which allows software to read and write longwords to 8-bit and 16-bit devices. Those features allow these computers to work with existing I/O software designed for the MC68030.

## Architecture

The PrimeTime IC also contains the sound control logic and the sound input and output buffers. There are three separate buffers—one for sound input and two for stereo sound output—so these computers can record sound input and process sound output simultaneously.

### DFAC II IC

---

The DFAC II custom IC contains the sound input processing devices. The DFAC II includes

- input AGC comparators
- antialias filtering
- A/D converter for input
- PWM converter for output

The DFAC II IC does not include the sound control logic and the input and output buffers; those are part of the PrimeTime IC.

For sound input, the DFAC II processes the signal from the sound input jack through a sound input amplifier with automatic gain control, an input filter, an A/D converter, and the necessary switching circuits. The DFAC II sends the resulting stream of digital sound data to the PrimeTime, which stores the data in its input buffer.

For sound output, circuits in the DFAC II take data from the sound output buffers and generate stereo pulse-width-modulated (PWM) signals. The DFAC II merges the sound playthrough signal with the PWM signals and sends the combined signals to an external stereo PWM converter IC. After low-pass filtering in the PWM converter, the signals go to the sound output jacks and to a separate amplifier for the built-in speaker. Inserting a plug into the sound output jack disconnects the internal speaker.

### Cuda IC

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The Cuda IC is a custom version of the Motorola MC68HC05 microcontroller. It includes

- the ADB interface
- programming interface for the DFAC II IC
- parameter RAM
- real-time clock

### Antelope IC

---

The Antelope IC is a custom IC containing the video CLUT (color look-up table) and DAC. The Antelope IC is pin and software compatible with the AC/DC custom IC used in the Macintosh Quadra 700 and 950, but does not support 24 bits per pixel or Apple convolution. For information about the number of bits per pixel provided on different video monitors, see “Video RAM Addresses” in the next section.

## Architecture

A separate pixel data bus handles data transfers from the VRAM to the Antelope IC. The pixel data bus is 32 bits wide and all data transfers are 32 bits at a time. The Antelope IC breaks each 32-bit data transfer into several pixels of the appropriate size—1, 2, 4, 8, or 16 bits per pixel. The Antelope IC does not support 24 bits per pixel.

The CLUT in the Antelope custom IC provides color palettes for 4-bit and 8-bit display modes. In 16-bit display mode, the CLUT is used to provide gamma correction for the stored color values. With a black-and-white or monochrome display mode, all three color components (R, G, and B) are the same.

## Address Maps

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The Macintosh LC 475 and Macintosh Quadra 605 computers support both 24-bit and 32-bit addressing. Figure 2-2 shows the relationship between the 24-bit addresses and the 32-bit addresses. The address map is similar to that of the Macintosh Centris 610 and 650.

**Note**

Developers should not use actual hardware addresses in applications but should always communicate with hardware devices by means of system software. ♦

### RAM Addresses

---

The first 1 GB of the address space is reserved for RAM. The actual amount of RAM installed can be from 4 MB to 36 MB. At startup time, a routine in the ROM determines the amount of RAM available and stores the size in a low-memory global variable.

### Video RAM Addresses

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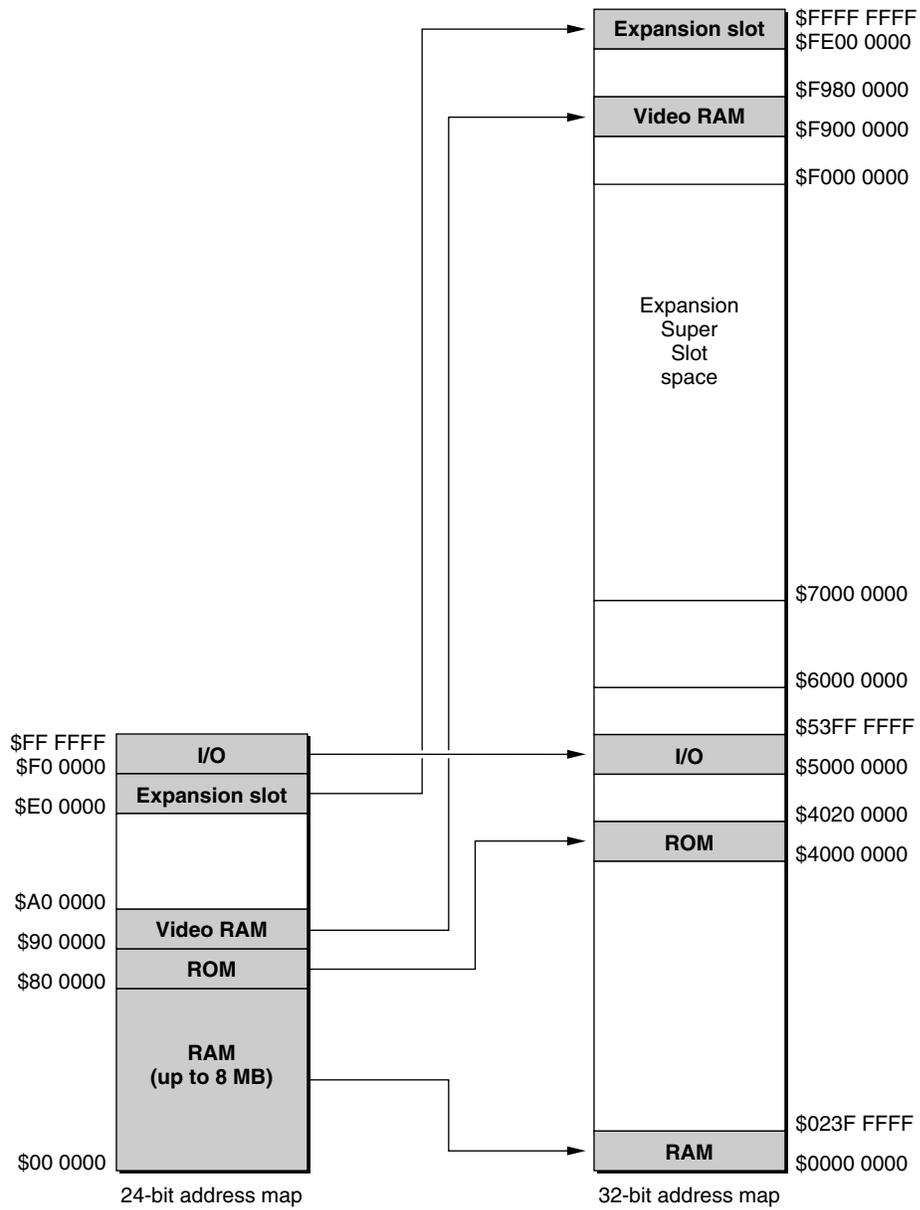
The Macintosh LC 475 and Macintosh Quadra 605 computers use separate VRAM to store the screen buffer. The VRAM occupies dedicated address space starting at \$F900 0000, as shown in Figure 2-2.

### Expansion Card Addresses

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The expansion card should use address space from \$FE00 0000 to \$FEFF FFFF, corresponding to NuBus slot \$E, or from \$E000 0000 to \$EFFF FFFF, corresponding to NuBus Super Slot \$E. For more information, see the section “Address Space” on page 40.

**Figure 2-2** Simplified 24-bit and 32-bit address maps



## Video Timing Parameters

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The Macintosh LC 475 and Macintosh Quadra 605 computers require an external video monitor. The monitor can be one of several different types and screen sizes, as listed in Table 2-1.

**Table 2-1** Monitors supported

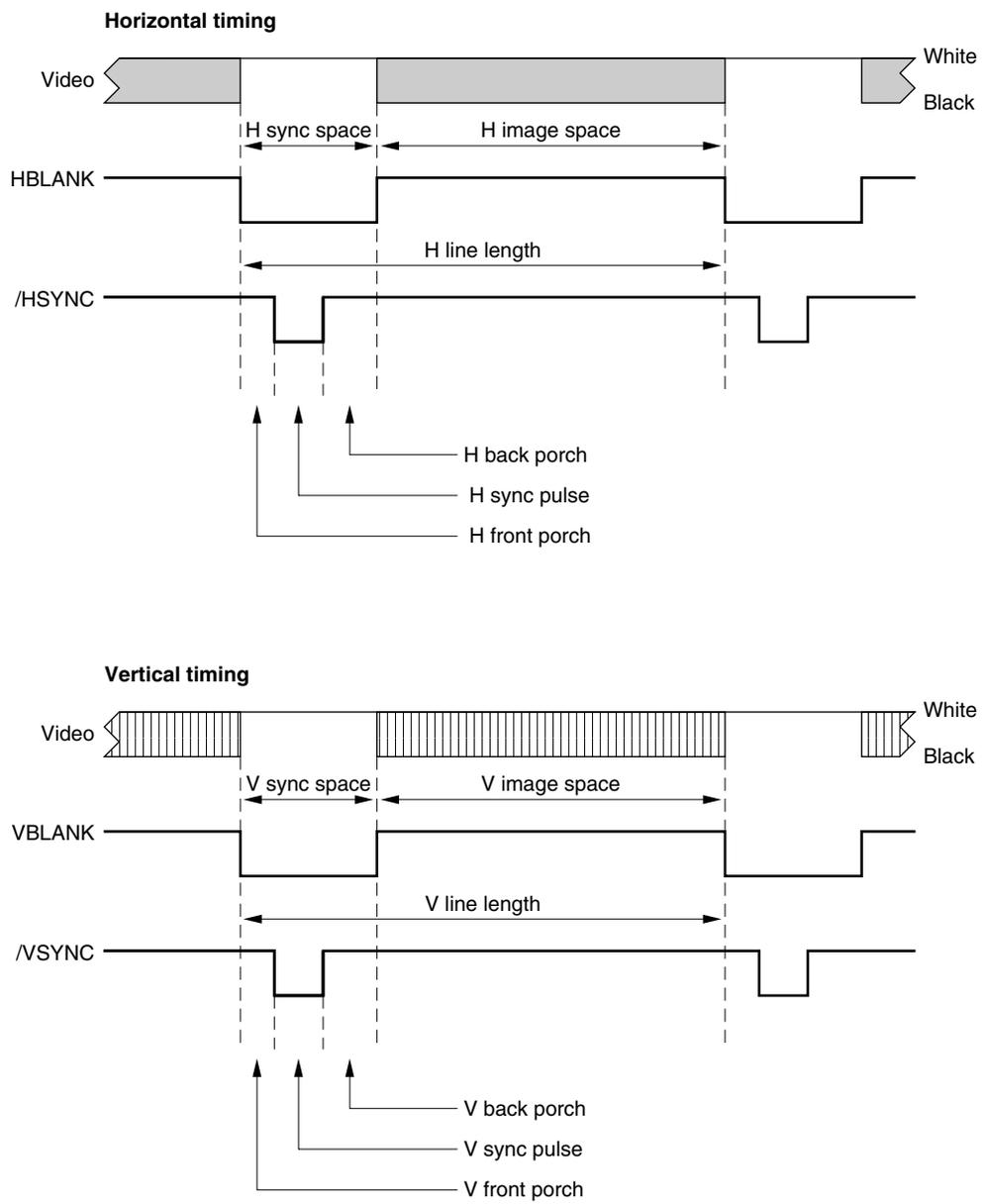
| Monitor type                | Monitor screen size |
|-----------------------------|---------------------|
| 12-inch color               | 512 × 384           |
| 12-inch monochrome          | 640 × 480           |
| 14-inch color               | 640 × 480           |
| 15-inch portrait            | 640 × 870           |
| 16-inch color               | 832 × 624           |
| 19-inch color               | 1024 × 768          |
| 21-inch color or monochrome | 1152 × 870          |
| NTSC or VGA                 | 640 × 480           |

Figure 2-3 shows simplified timing diagrams and identifies the horizontal and vertical timing parameters in a video signal. Table 2-2 and Table 2-3 list the values of those parameters for the different types of monitors.

### Note

When the Apple IIe Card for Macintosh is installed in the expansion slot, the computer generates an Apple IIe video display with 560 by 384 pixels. On the 12-inch color monitor, that display requires changes to the video timing, as shown in Table 2-2. ♦

**Figure 2-3** Video timing diagram



## Architecture

Table 2-2 shows the timing parameters for the smaller monitors listed: the 12-inch color monitor, the 14-inch color monitor, and a standard VGA monitor.

**Table 2-2** Video timing parameters for smaller monitors

| Parameter               | Monitor type and dimensions   |                                    |                               |                             |
|-------------------------|-------------------------------|------------------------------------|-------------------------------|-----------------------------|
|                         | 12-inch color<br>(512 by 384) | 12-inch color*<br>(Apple IIe card) | 14-inch color<br>(640 by 480) | VGA<br>(640 by 480)         |
| Dot clock               | 15.67 MHz                     | 17.234 MHz                         | 30.24 MHz                     | 25.18 MHz                   |
| Dot time                | 63.83 ns                      | 58.02 ns                           | 33.07 ns                      | 39.72 ns                    |
| Line rate               | 24.48 kHz                     | 24.48 kHz                          | 35.00 kHz                     | 31.47 kHz                   |
| Line time               | 40.85 $\mu$ s<br>(640 dots)   | 40.85 $\mu$ s<br>(704 dots)        | 28.57 $\mu$ s<br>(854 dots)   | 31.78 $\mu$ s<br>(800 dots) |
| Horizontal active video | 512 dots                      | 560 dots                           | 640 dots                      | 640 dots                    |
| Horizontal blanking     | 128 dots                      | 144 dots                           | 224 dots                      | 160 dots                    |
| Horizontal front porch  | 16 dots                       | 32 dots                            | 64 dots                       | 16 dots                     |
| Horizontal sync pulse   | 32 dots                       | 32 dots                            | 64 dots                       | 96 dots                     |
| Horizontal back porch   | 80 dots                       | 80 dots                            | 96 dots                       | 48 dots                     |
| Frame rate              | 60.15 Hz                      | 60.15 Hz                           | 66.67 Hz                      | 59.94 Hz                    |
| Frame time              | 16.63 ms<br>(407 lines)       | 16.63 ms<br>(407 lines)            | 15.00 ms<br>(525 lines)       | 16.68 ms<br>(525 lines)     |
| Vertical active video   | 384 lines                     | 384 lines                          | 480 lines                     | 480 lines                   |
| Vertical blanking       | 23 lines                      | 23 lines                           | 45 lines                      | 45 lines                    |
| Vertical front porch    | 1 line                        | 1 line                             | 3 lines                       | 10 lines                    |
| Vertical sync pulse     | 3 lines                       | 3 lines                            | 3 lines                       | 2 lines                     |
| Vertical back porch     | 19 lines                      | 19 lines                           | 39 lines                      | 33 lines                    |

\* The Macintosh LC 475 and Macintosh Quadra 605 computers can provide a 560-by-384 display on any size monitor; only the 12-inch monitor requires modified timing parameters to provide the 560-pixel display width.

## Architecture

Table 2-3 shows the timing parameters for the larger monitors: the 15-inch portrait monitor, the 16-inch color monitor, the 19-inch color monitor, and the 21-inch color monitor.

**Table 2-3** Video timing parameters for larger monitors

| Parameter               | Monitor type and dimensions      |                               |                                |                                |
|-------------------------|----------------------------------|-------------------------------|--------------------------------|--------------------------------|
|                         | 15-inch portrait<br>(640 by 870) | 16-inch color<br>(832 by 624) | 19-inch color<br>(1024 by 768) | 21-inch color<br>(1152 by 870) |
| Dot clock               | 57.28 MHz                        | 57.28 MHz                     | 80.00 MHz                      | 100.00 MHz                     |
| Dot time                | 17.46 ns                         | 17.46 ns                      | 12.5 ns                        | 10 ns                          |
| Line rate               | 68.85 kHz                        | 49.72 kHz                     | 60.24 kHz                      | 68.68 kHz                      |
| Line time               | 14.52 $\mu$ s<br>(832 dots)      | 20.11 $\mu$ s<br>(1,152 dots) | 16.60 $\mu$ s<br>(1,328 dots)  | 14.56 $\mu$ s<br>(1,456 dots)  |
| Horizontal active video | 640 dots                         | 832 dots                      | 1,024 dots                     | 1,152 dots                     |
| Horizontal blanking     | 192 dots                         | 320 dots                      | 304 dots                       | 304 dots                       |
| Horizontal front porch  | 32 dots                          | 32 dots                       | 32 dots                        | 32 dots                        |
| Horizontal sync pulse   | 90 dots                          | 64 dots                       | 96 dots                        | 128 dots                       |
| Horizontal back porch   | 80 dots                          | 224 dots                      | 176 dots                       | 144 dots                       |
| Frame rate              | 75.00 Hz                         | 74.55 Hz                      | 75.00 Hz                       | 75.08 Hz                       |
| Frame time              | 13.33 ms<br>(918 lines)          | 13.41 ms<br>(667 lines)       | 13.33 ms<br>(804 lines)        | 13.32 ms<br>(915 lines)        |
| Vertical active video   | 870 lines                        | 624 lines                     | 768 lines                      | 870 lines                      |
| Vertical blanking       | 48 lines                         | 43 lines                      | 36 lines                       | 45 lines                       |
| Vertical front porch    | 3 lines                          | 1 line                        | 3 lines                        | 3 lines                        |
| Vertical sync pulse     | 3 lines                          | 3 lines                       | 3 lines                        | 3 lines                        |
| Vertical back porch     | 42 lines                         | 39 lines                      | 30 lines                       | 39 lines                       |



# Expansion

---

## Expansion

The Macintosh LC 475 and Macintosh Quadra 605 computers have a slot for an I/O expansion card. This chapter describes the expansion slot and gives the specifications for an expansion card.

**IMPORTANT**

The expansion slot in the Macintosh LC 475 and Macintosh Quadra 605 computers is not a PDS (processor direct slot) because it is not connected directly to the main processor. PDS cards designed to interact with the main processor—to provide, for example, a RAM cache or an FPU—will not work in the expansion slot. ▲

## The Expansion Slot

---

The expansion slot in the Macintosh LC 475 and Macintosh Quadra 605 computers can accept either of two types of expansion cards: a 96-pin card similar to the PDS card used in the Macintosh LC II or a 114-pin card similar to the PDS card used in the Macintosh LC III.

The expansion connector in the Macintosh LC 475 and Macintosh Quadra 605 computers is mechanically the same as the expansion connector in the Macintosh LC III. It is essentially a 120-pin Euro-DIN connector with six pins removed to make a notch. The notch divides the connector into two sections: a 96-pin section that accepts the 96-pin connector used on expansion cards for the Macintosh LC II, and a separate 18-pin section for additional signals. See the section “Card Connectors” on page 40.

### Pin Assignments

---

Table 3-1 gives the pin assignments for the expansion connector. Pins 1 through 32 in all three rows (A, B, and C) correspond to the 96-pin section of the connector. Pins 33 and 34 in all three rows are missing—those pins correspond to the notch in the connector. Pins 35 through 40 in all three rows make up the 18-pin section of the connector.

Except for one signal, 16MASTER (on pin B31 and described in Table 3-2), the pin assignments on the 96-pin section of the extended PDS are the same as those on the PDS in the Macintosh LC II. On the Macintosh LC II, pin B31 is the Apple II video clock input.

**Note**

Signal names starting with a slash (/) are active when their signal lines are driven to a logical zero (0). ◆

**Note**

Under no circumstances should you use the Analog GND pin (Pin 1, Row B) for a digital ground on your expansion card. Doing so will cause digital noise to be coupled into the audio system, resulting in degraded sound quality. ◆

## Expansion

**Table 3-1** Pin assignments for the expansion connector

| Pin number | Row A       | Row B      | Row C       |
|------------|-------------|------------|-------------|
| 1          | SNDOUT      | Analog GND | /FPU.SEL    |
| 2          | /SLOTIRQ    | /R/W       | /DS         |
| 3          | /PDS.AS     | +5V        | /BERR       |
| 4          | /PDS.DSACK1 | +5V        | /PDS.DSACK0 |
| 5          | /HALT       | SIZ1       | SIZ0        |
| 6          | FC2         | GND        | FC1         |
| 7          | FC0         | CLK16M     | /RESET      |
| 8          | /RMC        | GND        | /SLOT.BG    |
| 9          | D31         | D30        | D29         |
| 10         | D28         | D27        | D26         |
| 11         | D25         | D24        | D23         |
| 12         | D22         | D21        | D20         |
| 13         | D19         | D18        | D17         |
| 14         | D16         | D15        | D14         |
| 15         | D13         | D12        | D11         |
| 16         | D10         | D9         | D8          |
| 17         | /BGACK      | /BR        | A0          |
| 18         | A1          | A31        | A27         |
| 19         | A26         | A25        | A24         |
| 20         | A23         | A22        | A21         |
| 21         | A20         | /IPL2      | /IPL1       |
| 22         | /IPL0       | D3         | D4          |
| 23         | D2          | D5         | D6          |
| 24         | D1          | D0         | D7          |
| 25         | A4          | A2         | A3          |
| 26         | A6          | A12        | A5          |
| 27         | A11         | A13        | A7          |
| 28         | A9          | A8         | A10         |
| 29         | A16         | A15        | A14         |
| 30         | A18         | A17        | A19         |

*continued*

## Expansion

**Table 3-1** Pin assignments for the expansion connector (continued)

| Pin number | Row A         | Row B         | Row C         |
|------------|---------------|---------------|---------------|
| 31         | /FANSPEED     | 16MASTER      | FC3           |
| 32         | +12V          | GND           | -5V           |
| 33         | (not present) | (not present) | (not present) |
| 34         | (not present) | (not present) | (not present) |
| 35         | A28           | /CPU.BG       | C16M          |
| 36         | A29           | +5V           | A30           |
| 37         | /CIOUT        | /CPU.AS       | /STERM        |
| 38         | /CBACK        | n. c.         | /CBREQ        |
| 39         | n. c.         | /CPU.DSACK0   | n. c.         |
| 40         | n. c.         | GND           | /CPU.DSACK1   |

All the signals on the expansion connector are capable of driving at least one TTL load (1.6 mA sink, 400  $\mu$ A source). Most of the signals are connected to other MOS devices on the main logic board; for those signals, the DC load on the bus signals is small. All the data lines (D0–D31) are connected to the PrimeTime custom IC so they have CMOS-type loads.

▲ **WARNING**

The SNDOUT pin must not be grounded; doing so will short-circuit the +5V power to the sound circuitry. If you don't use the SNDOUT pin, leave it unconnected. ▲

## Signal Descriptions

The expansion slot in the Macintosh LC 475 and Macintosh Quadra 605 computers is intended to be compatible with expansion cards designed for computers that use the MC68030 microprocessor (the Macintosh LC III and Macintosh LC 520 computers). Because the bus protocols of the MC68LC040 microprocessor are not the same as those of the MC68030, many of the signals on the expansion slot are not connected directly to the MC68LC040. Instead, those signals are connected to the PrimeTime custom IC, which emulates the MC68030 control and data buses.

The upper 30 address lines (A31–2) are connected directly to the MC68LC040 microprocessor. The I/O bus adapter logic in the PrimeTime IC provides the buffered data bus (IOD31–0) and the two lowest address lines (A1–0).

Table 3-2 describes the signals on the expansion connector.

## Expansion

**Table 3-2** Expansion connector signal descriptions

| Signal name                 | Signal description  |
|-----------------------------|---|
| A0–A31                      | Address lines.  |
| /BERR                       | Bus error; bidirectional signal indicating that an error occurred during the current bus cycle; when /HALT is also asserted, causes the bus cycle to be retried.  |
| /BGACK                      | Bus grant acknowledge; input signal indicating that external device has become bus master.  |
| /BR                         | Bus request; input signal indicating that external device is requesting to become bus master.   |
| /CBACK                      | CPU burst acknowledge; used with /STERM during a burst transfer to indicate that an individual element of a burst transfer is ready.  |
| /CBREQ                      | CPU burst request; used to initiate a quadruple longword burst transfer; tied to a 4.7K pull-up resistor.   |
| /CIOUT                      | Cache inhibit out signal from main processor, indicating that a second-level cache is allowed to participate in the current bus transaction; tied to a 300Ω pull-down resistor.   |
| C16M                        | Same signal as CLK16M.  |
| CLK16M                      | Independent clock running at 15.6672 MHz; provided for compatibility with Macintosh LC and LC II PDS cards.   |
| /CPU.AS                     | Address strobe; three-state signal indicating that an active bus transaction is occurring.  |
| /CPU.BG                     | Processor bus grant; signal from the external device can become bus master following completion of current processor bus cycle. This signal is electrically connected to the /SLOT.BG signal.   |
| /CPU.DSACK0,<br>/CPU.DSACK1 | Data strobe acknowledge signals; asserted by the addressed bus slave to end a bus transaction; also used to inform the master of the size of the slave's data port. These signals are electrically connected to the corresponding /PDS.DSACK signals. |
| D0–D31                      | Data lines.   |
| /DS                         | Data strobe. During a read operation, /DS is asserted when the external device should place data on data bus; during a write operation, /DS is asserted when the main processor has put valid data on the data bus.                                   |
| /FANSPEED                   | Increases the speed of the system fan when asserted; all expansion cards should tie this signal to ground (asserted).   |
| FC0–FC2                     | Function code used to identify address space of current bus cycle; tied to pull-up and pull-down resistors to indicate supervisor data space accesses.  |
| FC3                         | Additional function code bit, used to indicate that the software is running in 32-bit address mode. (As in the Macintosh LC II, the software always runs in 32-bit mode.)   |

*continued*

## Expansion

**Table 3-2** Expansion connector signal descriptions (continued)

| Signal name                 | Signal description  |
|-----------------------------|---|
| /FPU.SEL                    | Select signal for an optional MC68881 or MC68882 FPU; tied to a 4.7K pull-up resistor; never asserted by the logic board in a Macintosh LC 475 , or Macintosh Quadra 605 computer.  |
| /HALT                       | Used in conjunction with /BERR signal to terminate a bus cycle with a retry response; not used to stop processor execution.   |
| /IPL0–IPL2                  | Interrupt priority-level lines.   |
| /PDS.AS                     | Address strobe; synchronized to 16 MHz regardless of the actual processor speed; asserted only when a valid slot address is being generated by the bus master. When the card is the active bus master, the card may drive either this signal or /CPU.AS, but not both.  |
| /PDS.DSACK0,<br>/PDS.DSACK1 | Data strobe acknowledge signals; asserted by the addressed bus slave to end a bus transaction; also used to inform the master of the size of the slave's data port. These signals are electrically connected to the corresponding /CPU.DSACK signals.                   |
| /RESET                      | Bidirectional signal that initiates system reset.   |
| /RMC                        | Three-state output signal that identifies current bus cycle as part of an indivisible bus cycle such as a read-modify-write operation.  |
| /R/W                        | Read/write; three-state output signal that defines direction of bus transfer with respect to the current bus master; logical one (1) indicates a bus-master read, zero (0) indicates bus-master write.  |
| 16MASTER                    | Indicates the width of the data port when the card is alternate bus master. A logical one (1) indicates a 16-bit port; logical zero (0) indicates a 32-bit port. The signal is pulled high on the main logic board.   |
| SIZ0–SIZ1                   | Three-state output signals that work in conjunction with PrimeTime IC's dynamic bus sizing capabilities and indicate the number of bytes remaining to be transferred during current bus cycle.  |
| /SLOT.BG                    | Bus grant signal to the expansion card. A bus master card may take control of the system bus after all pending bus traffic has been completed (when /PDS.AS, /BGACK, and all /DSACK signals are inactive). This signal is electrically connected to the /CPU.BG signal. |
| /SLOTIRQ                    | Interrupt request line from the card; reported to the system by way of the SLOT.E request; when low, generates a level-2 interrupt if the slot interrupt enable bit is set.   |
| SNDOUT                      | Input to the speaker amplifier so that the card can drive the speaker independently of the main processor. This signal accepts only sound output by the method used on the original Apple II, using digital (TTL) levels.   |
| /STERM                      | Indicates termination of a synchronous transfer by a card using the MC68030 synchronous cycle.  |

## Expansion

The following signals on the expansion slot are permanently connected:

|             |                 |             |
|-------------|-----------------|-------------|
| /PDS.DSACK0 | is connected to | /CPU.DSACK0 |
| /PDS.DSACK1 | is connected to | /CPU.DSACK1 |
| /PDS.BG     | is connected to | /CPU.BG     |

Unlike those signals, the /PDS.AS signal is not connected to the /CPU.AS signal. The /PDS.AS signal is used only for addresses in the slot \$E address range; the /CPU.AS signal is used for addresses in expansion slot and Super Slot spaces \$6–\$8, \$A–\$D, and \$F (the slot \$9 address spaces are used for built-in video circuitry).

**IMPORTANT**

The expansion slot does not support MC68040 bus transfers. The expansion slot does not support a processor operating at a clock frequency other than 16 MHz. ▲

## Compatibility With Older Cards

---

While the expansion slot will accept PDS cards designed for the Macintosh LC II and LC III, some of those cards do not work. Cards that are incompatible with the expansion slot include

- cards designed to work as coprocessors with an MC68020 or an MC68030 or as replacements for those microprocessors. Such cards include accelerators, 68882 FPU cards, and cache cards. That type of card won't work because the microprocessor is different and because the slot signals are not connected directly to the microprocessor.
- cards with drivers that include incompatible code. Some drivers that do not obey Apple's programming guidelines don't work on machines that use the MC68040 microprocessor. For example, some of those drivers write directly to the cache control register in an MC68030. Such code won't work on an MC68040.
- cards with drivers that include code to check the `gestaltMachineType` value and refuse to run on a newer CPU. The idea seems to be to protect the users by refusing to run on a machine that the cards haven't been tested on. This is a general problem and applies to all new Macintosh models.

## The Expansion Card

---

The I/O expansion card for the Macintosh LC 475 and Macintosh Quadra 605 computers is approximately 3 inches wide by 5 inches long. It fits parallel to the main logic board and reaches to an opening in the back of the case (normally filled by a snap-out cover). The opening provides access to a 15-pin D-type connector on the card for external I/O.

## Expansion

## Mechanical Design

---

The I/O expansion card for the Macintosh LC 475 and Macintosh Quadra 605 computers is the same size and shape as the PDS card for the Macintosh LC III computer. The section “Foldouts” at the end of this developer note contains mechanical drawings showing the recommended design guidelines for the expansion card. Foldout 1 shows the maximum dimensions of the expansion card and the location of the expansion connector. Foldout 2 provides component height restrictions for the expansion card. Foldout 3 shows how the card is installed on the main logic board.

## Card Connectors

---

The custom 114-pin PDS connector on the computer’s main logic board accepts either a 96-pin or 120-pin standard Euro-DIN connector. You can order connectors meeting Apple specifications from Amp Incorporated, Harrisburg, PA 17105 or from Augat Incorporated, Interconnect Products Division, P. O. Box 779, Attleboro, MA 02703. Refer to *Designing Cards and Drivers for the Macintosh Family*, third edition, for more information about those connectors.

## Power for the Card

---

The maximum current available at each supply voltage is shown in Table 3-3. The card must not dissipate more than 4 W total; for example, if the card uses the maximum current at -5 V and +12 V, it must not use more than 300 mA from the +5 V supply.

**Table 3-3** Power available for the expansion card

| Voltage | Current |
|---------|---------|
| +5      | 800 mA  |
| -5      | 20 mA   |
| +12     | 200 mA  |

▲ **WARNING**

Cards dissipating more than 4 watts may overheat and damage the computer’s circuitry or cause it to become inoperable. ▲

## Address Space

---

The expansion card’s address space depends on the memory addressing mode. In 24-bit mode, the card appears in address space \$E0 0000–\$EF FFFF; in 32-bit mode, the card appears in physical address spaces \$E000 0000–\$EFFF FFFF and \$FE00 0000–\$FEFF FFFF. To match the conventions used by the Slot Manager, software should address the card as if it were in slot space \$E: either the 16 MB slot space \$FE00 0000–\$FEFF FFFF or the super slot space \$E000 0000–\$EFFF FFFF.

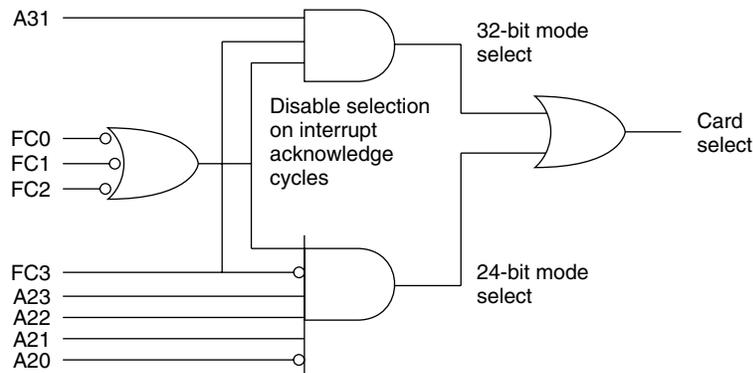
## Expansion

The expansion card must generate its own select signal from the address and function code signals on the connector. The card select signal must be disabled when FC0, FC1, and FC2 are all active; that condition corresponds to a function code of 111 (CPU space). Figure 3-1 shows a typical logic circuit for generating the card select signal.

**IMPORTANT**

To ensure compatibility with future hardware and software, you should minimize the chance of address conflicts by decoding all the address bits. To ensure that the Slot Manager recognizes your card, the card's declaration ROM must reside at the upper address limit of the 16 MB address space (\$FE00 0000–\$FEFF FFFF). ▲

**Figure 3-1** Generating the card select signal



## Bus Master on a Card

The expansion slot will support a card with an MC68020 or MC68030 bus master. The PrimeTime custom IC controls bus arbitration between the card's bus master and the MC68LC040 microprocessor so that either bus master will eventually obtain the bus. The MC68020 or MC68030 will obtain the I/O data bus and the address bus. The MC68LC040 will obtain the processor data bus and the address bus. Because there is only one address bus, there can be only one bus master at a time.

Asynchronous transfers are the preferred method for data transfers to and from an expansion card. When an expansion card contains an active bus master, the PrimeTime IC terminates successful data transfers using the DSACK signals. A slave on the expansion card can also terminate a transfer using DSACK signals.

The PrimeTime IC can never be a synchronous slave on the I/O bus, so PrimeTime cannot terminate data transfers as a slave using /STERM. On the other hand, a bus slave on an expansion card can terminate a 32-bit wide synchronous transfer using /STERM. PrimeTime supports /STERM terminations as a master on the I/O bus, and all transfers from PrimeTime to the expansion slot are based on the 16 MHz clock.



# Software

---

## Software

The first part of this chapter describes the software in the ROM of the Macintosh LC 475 and Macintosh Quadra 605 computers. The second and third parts describe the system software and the Screen driver that support the new features of those computers.

## ROM Software

---

The ROM in the Macintosh LC 475 and Macintosh Quadra 605 computers is based on the ROM for the Macintosh Centris 610 and 650 models with the necessary changes to support machine-specific hardware.

The sections that follow describe the following changes in the ROM:

- modularity
- machine identification
- new memory controller
- new memory maps
- new video ICs
- new sound IC and primitives
- ADB and power management

### Modularity

---

The ROM has been designed to detect optional features and configure the software appropriately. The optional features include an FPU in the MC68040 in the main processor socket.

### Machine Identification

---

The ROM includes new tables and code for identifying the machine.

Applications can find out which computer they are running on by using the Gestalt Manager routines; see *Inside Macintosh*, Volume VI. The 'gestaltMachineType' value for the Macintosh LC 475 computer is 89 (\$59); for the Macintosh Quadra 605 computer, it is 94 (\$5E).

Software

## New Memory Controller

---

The ROM code has been modified to support the MEMCjr custom IC, which has different features and a different programming interface from the MEMC IC. Unlike the MEMC, the MEMCjr supports 1 MB and 2 MB SIMMs, as well as the larger sizes.

## New Memory Maps

---

The ROM code has been modified to support the memory addressing used by the Macintosh LC 475 and Macintosh Quadra 605 computers. ROM code determines the size of RAM and sets up the MMU to make the RAM addresses contiguous. The ROM includes descriptions of the memory space needed for setting up the MMU.

The ROM code also creates the physical-space tables each computer needs in order to run virtual memory. To be able to run with virtual memory active, these computers use the 32-bit Memory Manager and run in 32-bit mode.

The ROM adds an MMU table that provides access to the video frame buffer in 24-bit address space so that the Apple IIe card will work on these machines.

## New Video ICs

---

The video frame-buffer controller in the MEMCjr custom IC is similar to the DAFB IC used in the Macintosh Quadra and Centris models. The video driver code has been changed to accommodate the differences between the MEMCjr IC and the previous MEMC IC and to support a new video clock generator IC.

## New Sound IC and Primitives

---

The sound primitives for the Macintosh LC 475 and Macintosh Quadra 605 computers are the same as those in the Macintosh LC 520 computer. The primitives have been integrated into the main ROM code.

## ADB and Power Management

---

The CUDA IC provides the ADB interface, parameter RAM, and power management. The ROM code to support the CUDA IC was originally developed for the Macintosh LC 520 computer.

When the user chooses Shut Down from the Special menu, a dialog appears telling the user that it is now safe to shut off the computer. The user then turns off the power by pressing the switch on the back.

## System Software

---

The Macintosh LC 475 and Macintosh Quadra 605 computers require System 7.1 or a later version of system software. The disk labeled “Install Me First” includes a system enabler file that contains the resources the system needs to start up and initialize those computers.

The system software includes the following new features:

- system enabler for these machines
- enhanced QuickDraw

### System Enabler

---

Starting with the international release of System 7.1, each reference release of the Macintosh system software supports a new startup extension, the system enabler. A **system enabler** is a software resource that is able to perform the correct startup process for one or more Macintosh computers.

As soon as the system software on disk takes over the startup process, it searches for all system enablers that can start up the particular machine. Each system enabler contains a resource that specifies which computers it is able to start up and the time and date of its creation. If the system software finds more than one enabler for the particular computer, it passes control to the one with the most recent time and date.

In general, the system enabler included in each reference release of system software is able to start up all previous computers. The system enabler that accompanies a later computer will be able to start up that computer, possibly using resources from the previous reference release.

### Enhanced QuickDraw

---

Like other Macintosh models that use the MC68040 microprocessor, the Macintosh LC 475 and Macintosh Quadra 605 computers have code in the system enabler to modify some QuickDraw drawing routines. The code provides new QuickDraw routines that take advantage of the MOVE16 instruction in the MC68040 to speed up vertical scrolling and solid fills.

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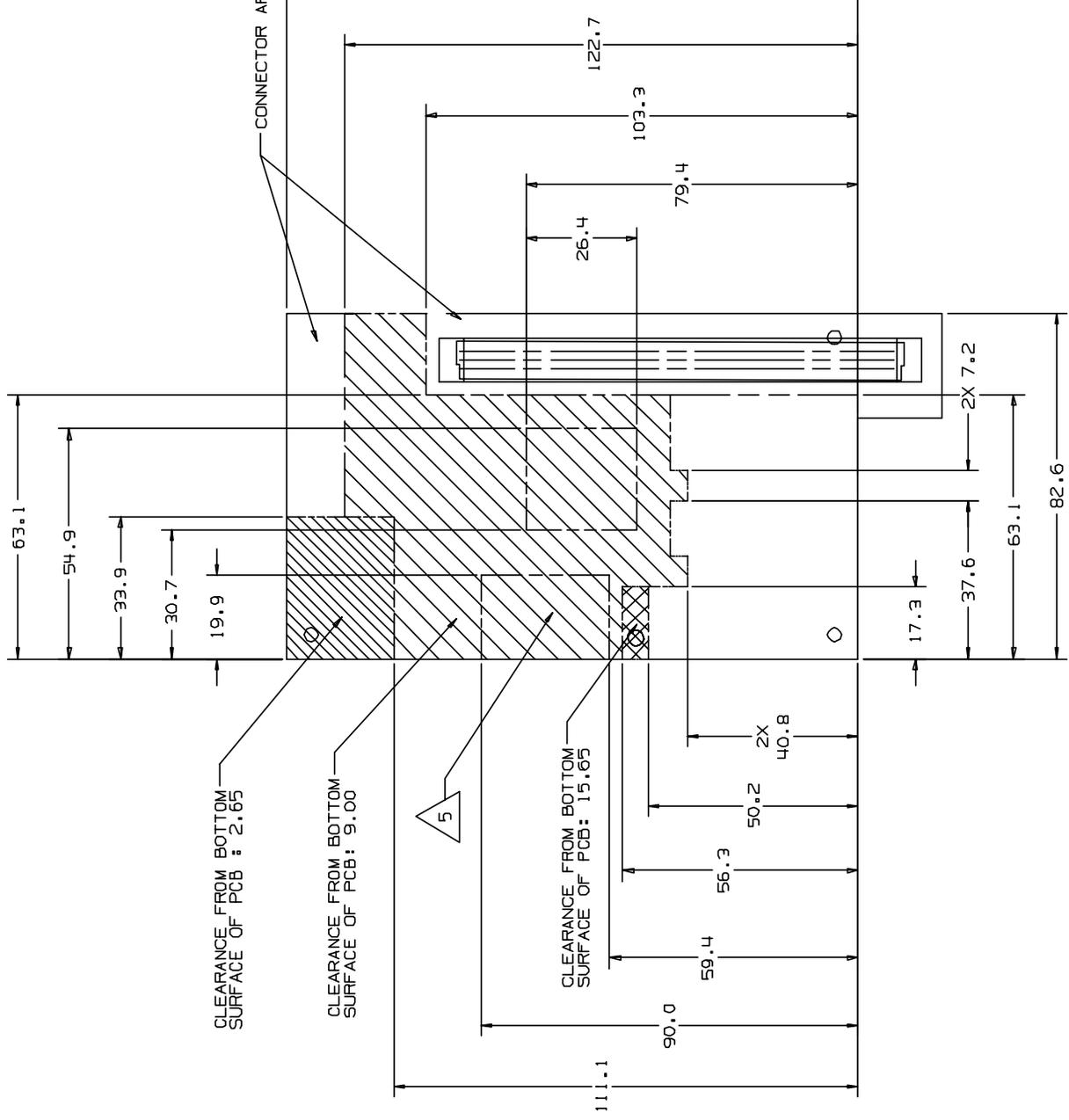


# Foldouts

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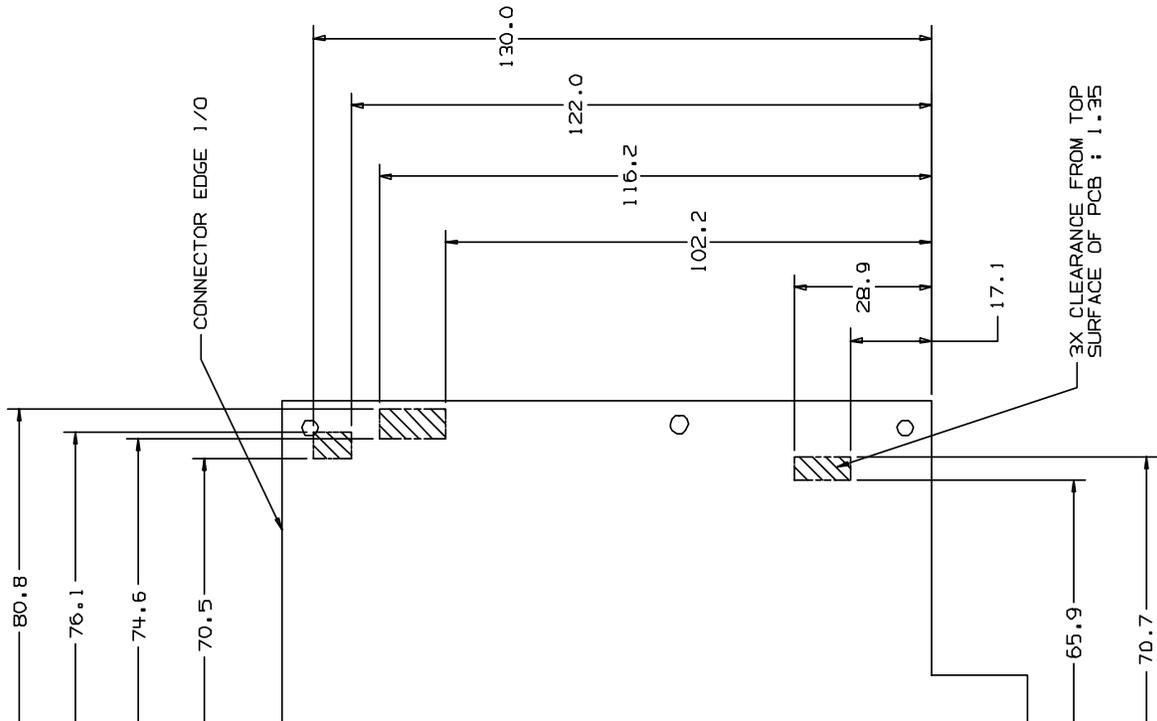




UNLESS NOTED CLEARANCE = 6.25MM

DETAIL **B**

BOTTOM SIDE  
 COMPONENT HEIGHT RESTRICTION ZONES  
 COMPONENT SIDE OF BOARD



UNLESS NOTED CLEARANCE = 8.0

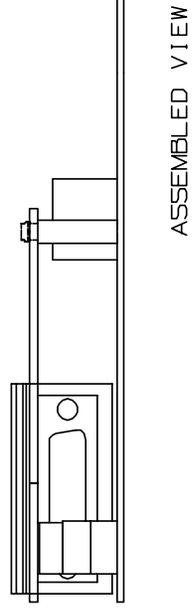
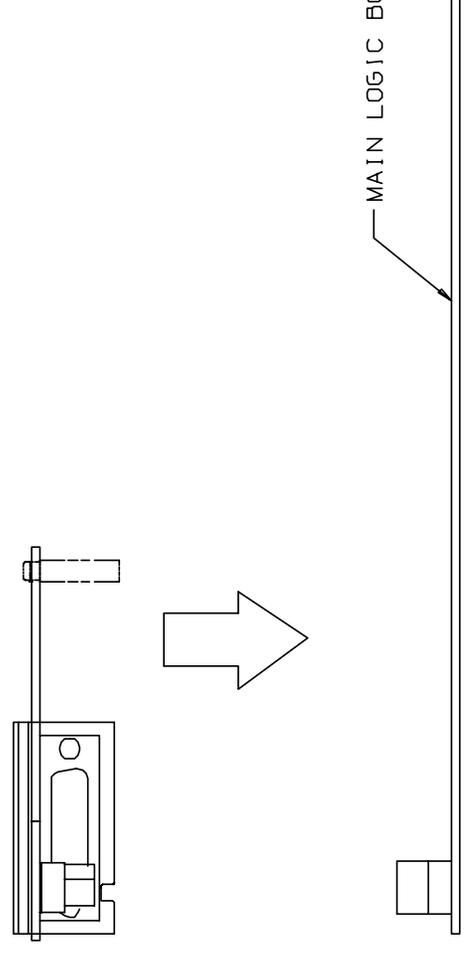
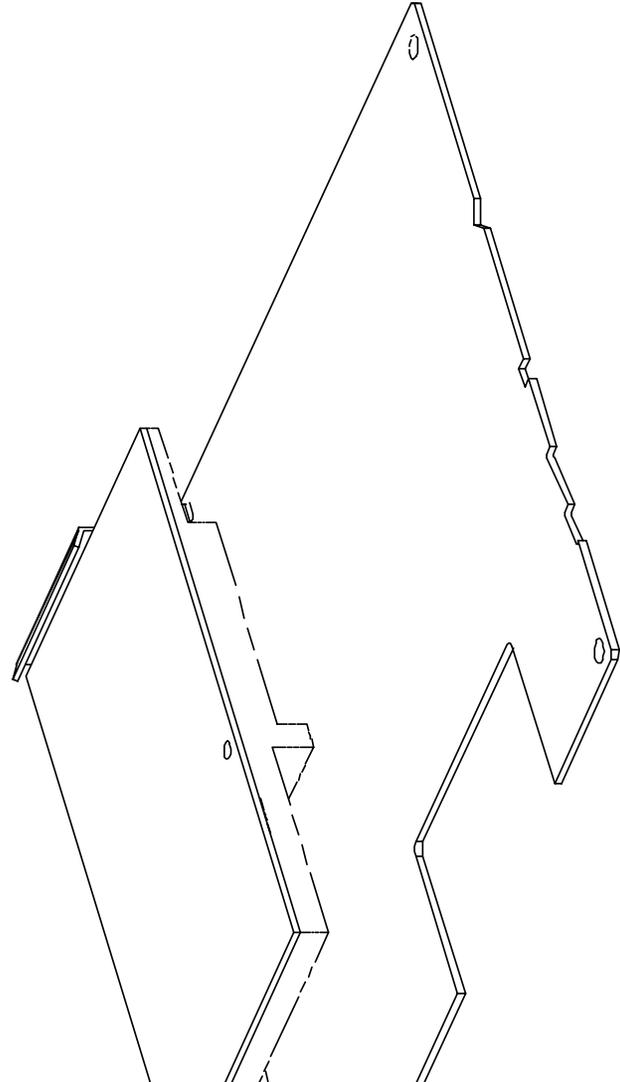
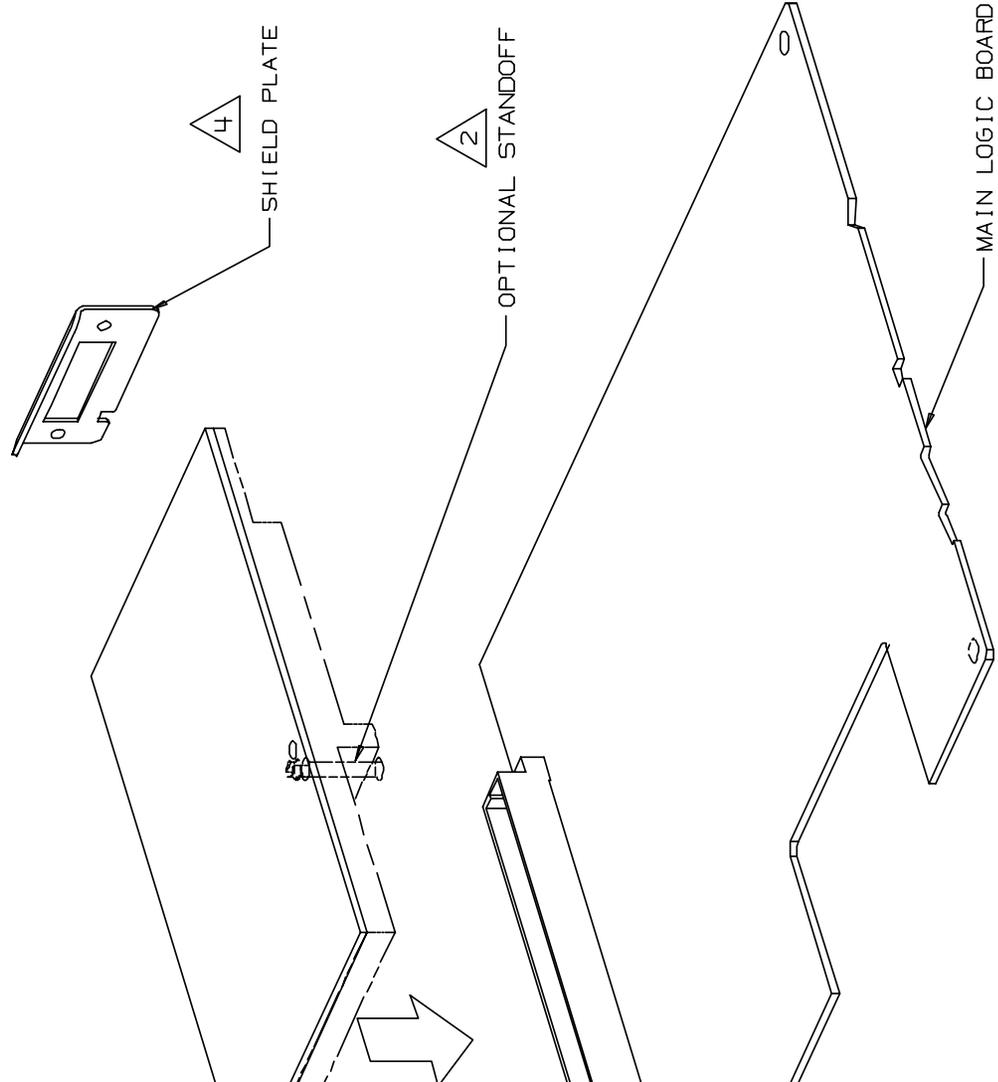
DETAIL **A**

TOP VIEW  
 COMPONENT HEIGHT RESTRICTION ZONES  
 SOLDER SIDE OF BOARD

FOLDOUT 2

Expansion card component

062-0487-B



**FOLDOUT 3**

Expansion card assembly

**062-0487-B**

ASSEMBLED VIEW